Photodetection characterization of SPADs fabricated in 0.35μm PIN photodiode and high voltage CMOS technologies

S. S. Kohneh Poushi, H. Mahmoudi, M. Hofbauer A. Dervic H. Zimmermann
Institute of Electrodynamics, Microwave and Circuit Engineering, Vienna University of Technology, Vienna 1040, Austria
saman.kohneh@tuwien.ac.at

***Abstract*—Given the doping profiles available in different CMOS technologies, different single-photon avalanche diode (SPAD) structures could be designed. A good insight into the effect of various doping profiles on the electric field distribution within the device is crucial for optimizing the photodetection performance. In this paper, we present an experimental and simulation characterization of the photon detection probability (PDP) for two reach-through SPADs with different doping profiles, and study the effect of the electric field distribution on the PDP performance. We use a comprehensive model to evaluate the PDP up to an excess bias voltage of 13.2V. In addition, it is shown that the SPAD with a thicker high-field region, despite having the lower maximum value of the electric field, shows higher carrier avalanche triggering probabilities and, consequently, a higher PDP (67% at 13.2 V excess bias and a wavelength of 642 nm). The PDP at the wavelength of the absolute transmission maximum of the isolation and passivation stack at 665 nm is even 84% at 13.2 V excess bias. The presented results and discussions can offer a better insight to the designer to achieve higher PDP for other SPAD structures by optimizing the electric field profile using doping modifications.**

***Keywords*—Single-photon avalanche diode (SPAD), Photon detection probability (PDP), Electric field distribution**

I. INTRODUCTION

Due to the possibility of single-photon detection and CMOS compatibility, single-photon avalanche diodes (SPADs) are promising optical detectors in different sensor and imaging applications such as visible light communication, time-of-flight sensing, quantum cryptography, and biomedical microscopy [1]–[6]. CMOS integrated SPADs use an n+/p-well or a p+/n-well junction where a strong electric field can be formed over a shallow region at the p/n interface (multiplication region) if the device is biased above its breakdown voltage [7]–[9]. The absorption of a single photon can generate an electron-hole pair, which can reach the multiplication region and trigger a self-sustaining avalanche due to the impact ionization effect. As a result, a macroscopic current pulse is generated that can be detected by simple electronic circuits.

The sensitivity of SPADs is evaluated by the probability that an incident photon generates a detectable avalanche event, known as photon detection probability (PDP). The PDP performance is affected by the optical transmission through the isolation and passivation stack, the absorption profile, and the probability that a photo-generated carrier triggers a self-sustaining avalanche event. There have been various approaches in terms of design concepts to improve the photodetection probability by implementing an antireflection coating [10], by adding microlenses [11] and by manipulating the depth of the multiplication zone [12], [13].

Here we compare the electric field distribution by using different doping profiles in two CMOS SPADs and study the effect of the electric field distributions on the PDP performance. In fact, this corresponds to a kind of electric-field engineering by comparing two CMOS processes. In order to characterize the PDP, the comprehensive simulation and modeling approach presented in [14] is implemented, which provides good insight into the effect of different parameters on PDP performance that is not possible to achieve by pure experiments. Accordingly, we compare the two SPADs' measured and simulated PDP spectra and explain the results, especially how the electric field affects the avalanche triggering probability as a key factor for PDP. Furthermore, the effect of increasing the excess bias on the PDP performance is studied.

The remainder of this paper is organized as follows. Sec. II explains the SPADs' structure as well as the simulation and modeling approach. In Sec. III, the PDPs of the two SPADs are compared, and the results are discussed based on TCAD simulations. Finally, the paper is concluded in Sec. IV.

II. DEVICE STRUCTURE AND SIMULATION APPROACH

A. SPAD structures

Fig. 1 shows the cross-sections of an n^+/p-well SPAD fabricated in the 0.35 μm pin-photodiode CMOS technology (SPAD1) and of a 0.35 μm high-voltage CMOS SPAD (SPAD2) of X-FAB Semiconductor Foundries. It should be mentioned, that the pin-photodiode CMOS process is a standard mixed-signal CMOS process and also offers a bipolar transistor process module. SPAD1 includes a shallow n^+ and a p-well region formed on a p-doped epitaxial layer (p- epi) with a thickness of $\sim$12 μm as well as a doping concentration of $\sim 2\times10^{13}$ cm^{-3} [7]. SPAD1 is a so-called reach-through SPAD [15] offering a

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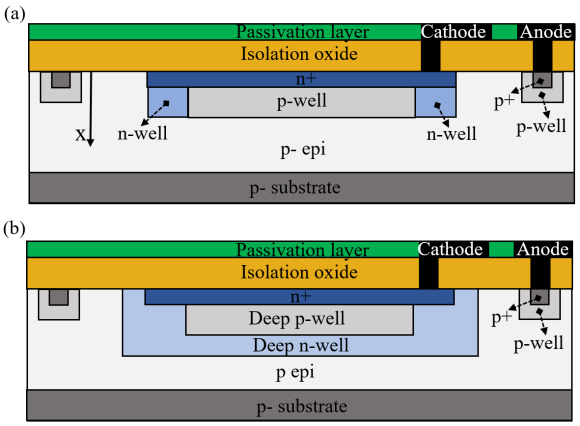

Fig. 1: Cross section of the n^+/p-well SPAD in pin-photodiode CMOS (SPAD1) (a) and of the HV CMOS SPAD (SPAD2) (b) (both figures not to scale).

thick absorption region. In order to avoid premature edge breakdown, the diameter of the p-well is smaller than that of the n^+ cathode. SPAD2 uses a deep p-well, a deep n-well and the p-type epi layer with a doping concentration of $\sim 1\times10^{15}$ cm^{-3}. The deep n-well compensates part of the deep-p-well doping and part of the p-epi doping to achieve a reach-through SPAD with a thick fully depleted absorption region in the epi layer [16].

By increasing the applied reverse bias, the space-charge region expands from the p/n-junction through the p-well or deep p-well towards the substrate. Therefore, a high electric field is formed below the junction inside the p-well or deep p-well, which generates the multiplication region, while a weaker electric field is placed over the epitaxial layers, which serve as the absorption region. However, for reverse biases higher than a specific level, the devices enter a "fully-depleted" condition, which means the entire thickness of the epitaxial layers is depleted. SPAD1 reaches full depletion at about 19V, whereby its breakdown voltage is ~25 V. In SPAD2, a deep n-well region covers the n^+/deep-p-well to decrease the effective doping concentration of the deep p-well. As a result, the breakdown voltage increases to 67 V, which guarantees that the p epi layer gets fully depleted also far below the breakdown voltage. Accordingly, both SPADs comprise the thick absorption zone, making them more efficient at longer wavelengths (i. e. for red and infrared light).

The whole surface of both CMOS SPADs is covered by a thick isolation-oxide and passivation stack, and therefore the incident photons reach the silicon after passing through these layers. As explained in [14], the formation of standing waves in this stack causes maxima and minima in the PDP spectrum.

B. PDP Modeling

PDP quantifies the ability of the SPAD to detect photons, and it is defined as the ratio of the number of detected photons to the total number of incident photons. To calculate the PDP, one has to consider the probability of a photon entering the silicon as not every incident photon is transmitted into the silicon due to the non-zero reflection coefficient. In addition, as not every photo-generated carrier has a chance to initiate a self-sustaining avalanche, the avalanche triggering probability (P_{av}) is essential to be taken into account. Accordingly, the PDP is a function of two probability terms, the photon absorption probability (P_{ab}) and P_{av}, and obtained as

$$\mathrm{PDP}(\lambda) = \int_0^{x_{si}} \mathrm{P_{ab}}(\lambda, x) \times \mathrm{P_{av}}(x) dx. \qquad (1)$$

Where $\mathrm{P_{ab}}(\lambda, x)$ is the photon absorption probability distribution inside the silicon at any x multiplied by the optical transmission into the silicon, extracted from electromagnetic simulations using CST Microwave Studio [17]. It is noteworthy that this term is affected by the layers deposited above the sensitive area. Ref [14] explains in detail how to obtain this term and to use it in the model.

$\mathrm{P_{av}}(x)$ is the total avalanche triggering probability (ATP), representing the probability that either an electron or a hole at any depth (x) triggers a self-sustaining avalanche event, obtained as

$$\mathrm{P_{av}} = (\mathrm{P_e} + \mathrm{P_h} - \mathrm{P_e P_h}) \times P_{\mathrm{diff}}(x), \qquad (2)$$

where $P_{\mathrm{diff}}(x)$ is the probability that a carrier generated in the neutral region diffuses into the depletion region. $\mathrm{P_e}$ and $\mathrm{P_h}$ are respectively the electron and hole avalanche triggering probabilities, given by solving the following coupled equations

$$\begin{aligned} \frac{\partial P_\mathrm{e}}{\partial x} &= (1 - P_\mathrm{e})\gamma_\mathrm{e}(P_\mathrm{e} + P_\mathrm{h} - P_\mathrm{e}P_\mathrm{h}), \\ \frac{\partial P_\mathrm{h}}{\partial x} &= (1 - P_\mathrm{h})\gamma_\mathrm{h}(P_\mathrm{e} + P_\mathrm{h} - P_\mathrm{e}P_\mathrm{h}), \end{aligned} \qquad (3)$$

where γ_e and γ_h are respectively the electron and hole impact ionization coefficients, which strongly depend on the electric field. Here, we perform Geiger-mode device simulations using SILVACO Atlas [18] to obtain the avalanche triggering probability for both SPADs.

III. Comparison of Simulation and Measurement

The results of measurement and simulation of the PDP spectrum at an excess bias of 6.6 V are compared in Fig. 2. There is a very good agreement between simulated and measured results, which guarantees that the simulation and modeling approach captured the key optical and electrical

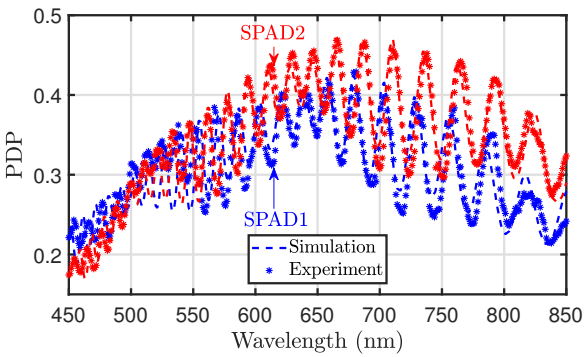

Fig. 2: PDP spectra based on experiment (dotted) and simulation (dashed lines) at an excess bias of 6.6 V.

parameters, and therefore, it is reliable to study the PDP behavior using those parameters.

It can be observed that the PDP of SPAD2 at long wavelengths ($\lambda \gtrsim 580$ nm) is higher than that of SPAD1. From this fact, we have to conclude that bipolar SPAD receivers should use yellow or green light to exploit the advantages of bipolar transistors because the higher PDP for red or near-infrared light of high-voltage CMOS SPAD receivers may excel their overall receiver performance [19], [20]. As both SPADs are covered by similar layers (isolation and passivation stack), it is expected that they should have similar optical behavior. Then, according to the model, one can say that the difference in the PDP of the two SPADs is mainly due to their different avalanche triggering probabilities. The ATP strongly depends on the electric field and the ionization coefficient distribution. Accordingly, we performed TCAD simulations to calculate these parameters and, consequently, the ATP profile for both SPADs.

Fig. 3(top) illustrates the electric field distributions (vertical cross-section at the center) in the depth interval x=[0;2] μm of the two SPADs at an excess bias voltage of 6.6 V. As shown, an electric field is formed in both structures with very high strength at the n^+/p-well or n+/deep-p-well junction and in the multiplication region and with a lower amplitude in the absorption region. A photo-generated electron-hole pair in the depleted region is promptly separated by the electric field, and then the minority carrier (i.e. electron or hole depending on where the photon is absorbed) drifts towards the multiplication region. The high electric field in the multiplication region provides sufficient energy to carriers for impact ionization.

By a close look into the electric field profile, we observe that the maximum value of the electric field in SPAD2 is slightly lower than that of SPAD1, however, its high-field region is wider. As a result, the electron and hole ionization coefficients in SPAD2 show a wider distribution but with a smaller maximum value compared to SPAD1 as shown in Fig. 3(middle). The ionization coefficient at any x represents the mean number of electrons/holes generated by a carrier per unit length of the path in the direction of the field. Therefore, in SPAD2 the ionization events occur in a thicker region, however, its multiplication rate is lower than that of SPAD1.

Accordingly, the electron and hole avalanche triggering probability distributions (Fig. 3(bottom)) for both SPADs as a function of depth (x) are calculated according to the ionization coefficient profiles. The probability that a photo-generated carrier triggers an avalanche event depends on where it is born. A carrier generated at the beginning of the multiplication zone is more likely to initiate an avalanche event than the one generated close to the end of the multiplication region. Because it travels a longer distance in the presence of the high electric field and therefore, it has a higher chance of initiating an avalanche event. It is interesting to note that even though the avalanche process happens only in the multiplication region, the minority

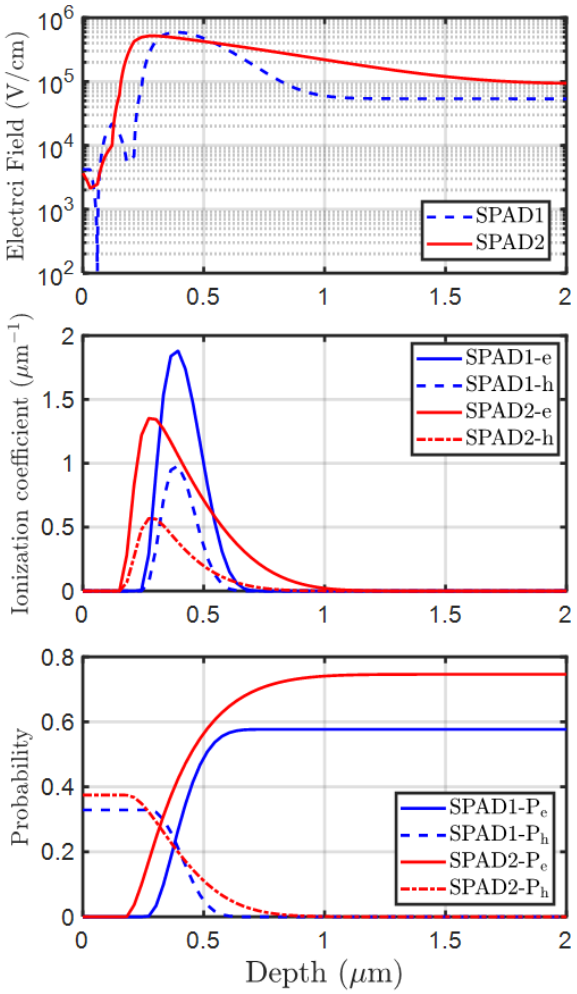

Fig. 3: Extracted distributions of electric field (top), electron and hole ionization coefficients (middle), and electron and hole avalanche triggering probabilities (bottom) as a function of the depth (x) at an excess bias of 6.6 V.

carrier generated outside the multiplication region reaches this area and passes across the whole multiplication region. As a result, the avalanche triggering probability shows the maximum value for the minority carrier outside the multiplication region while it is zero for the majority carrier.

Fig. 3(bottom) provides a comparison of P_e and P_h of the two SPADs. According to this figure, P_e and P_h of SPAD2 are higher than that of SPAD1, despite having the lower maximum value of carriers ionization coefficient. This is because the ionization coefficient profile and, consequently, the multiplication region of SPAD2 is thicker than that of SPAD1, as to acquire sufficient energy to create an avalanche event, not only the absolute value of the ionization coefficient but also the thickness of the multiplication region plays a significant role. In fact, there will be a higher number of possible collisions in the wider high-field region, leading to higher avalanche triggering probabilities. In addition, the maximum value of P_h is smaller than the maximum value of P_e due to the fact that the impact ionization coefficient associated with the holes is smaller compared to that of the electrons.

Now, we can justify the above-discussed PDP spectrum by comparing the avalanche triggering probabilities of the two SPADs (Fig. 3). The higher PDP of SPAD2 compared to SPAD1 at the long wavelengths is due to the fact that a significant portion of the total transmitted photons at long wavelengths is absorbed in larger depths (below the multiplication region) where P_e of SPAD2 is higher than that of SPAD1. However, photons of short wavelengths are more likely to be absorbed in or above the multiplication region, where the difference between P_e and P_h of both structures is smaller and, therefore, the PDP of both SPADs is expected not to have a significant difference at short wavelengths. To provide a more general picture, Fig. 4 compares the photon absorption probability as a function of depth x inside the silicon for a short and a long wavelength of the spectrum. It can be seen that at the short wavelength, a considerable portion of the transmitted photons are absorbed in or above the multiplication region while the photon absorption probability of the long wavelength is wider over the depth.

In order to show how the increase in the electric field affects the performance of PDP, Fig. 5 shows the PDP as a function of the excess bias voltage for a wavelength of 642 nm. For SPAD1, the integrated quenching/resetting circuit presented in [21] was employed to apply excess biases up to 13.2 V. However, for SPAD2 the excess bias was swept up to 6.6 V by the quenching/resetting circuit presented in [7]. It is expected that by increasing the excess bias, a stronger electric field is applied across the multiplication region, increasing both P_e and P_h and thus enhancing the PDP.

In addition, the electric field in the multiplication zone shows a linear increment with the excess bias voltage, leading to an almost linear increase in PDP with the excess bias. The somewhat sub-linear increase of the PDP of SPAD2 with the excess biases above 9 V indicates slight saturation effects. It should be mentioned that the non-linear behavior of the PDP at low excess biases is due to the effect of the readout circuit, which is not considered in the presented SPAD modeling and simulation approach. Furthermore, as the simulated results fit the measured data with an excellent agreement, we can make a prediction

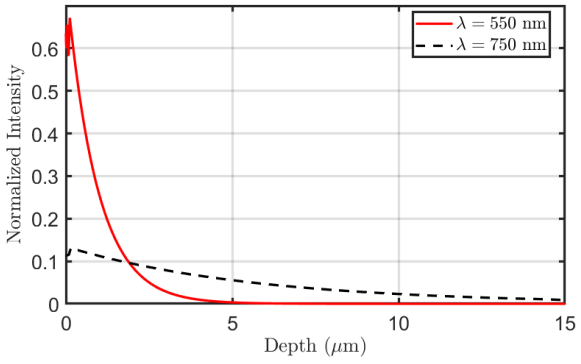

Fig. 4: Normalized light intensity as a function of depth x for a short (λ=550 nm), and a long (λ=750 nm) wavelength.

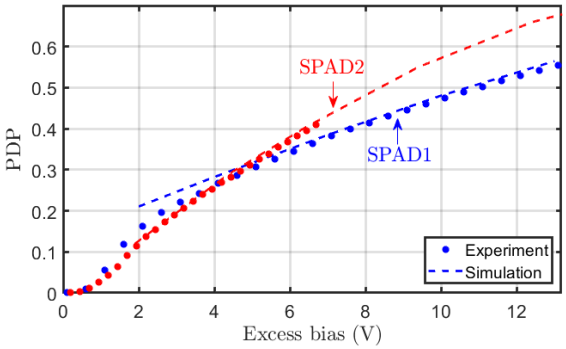

Fig. 5: Measured (dotted) and simulated PDP (dashed lines) as a function of excess bias at a wavelength of 642 nm.

of the PDP of SPAD2 at higher excess bias as shown in Fig. 5. At the excess bias of 13.2 V, we expect that a PDP of 67% will be achieved for SPAD2 while the PDP of SPAD1 is 55%. At the wavelengths of the absolute maxima of 665 nm and 676 nm in Fig. 2, respectively, the calculated PDPs for V_{ex}=13.2 V of SPAD1 and SPAD2 are $\sim 84\%$ and $\sim 65\%$.

IV. Conclusion

The experimental and simulation study is presented to evaluate how the electric field distribution inside the structure influences the PDP performance of CMOS-based SPADs. It is demonstrated that the SPAD with a thicker high-field region, despite having the lower maximum value of the electric field, shows a better PDP performance. Thus, the more complex high-voltage CMOS process offers a better PDP performance for the red and near-infrared spectral ranges as a standard mixed-signal or digital CMOS process of the same minimum structure size. The results and discussions presented in this paper can be used in other SPAD structures to improve the PDP performance by manipulating the electric field distribution using doping modifications.

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