Monolithic Receiver with Nine Single-Photon Avalanche Diodes

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***Abstract* – An optical receiver containing nine single-photon avalanche diodes (SPADs) and nine active quenching circuits is presented. This optical receiver was fabricated in a 0.35µm high-voltage CMOS technology without any process modifications. The SPADs avoid the excess noise of linear-mode avalanche diode receivers and allow for a better optical sensitivity. With 680 nm light, the 9-SPAD receiver achieves a sensitivity of -56.8 dBm for a bit error ratio of 2×10^{-3} at a data rate of 50 Mb/s. Compared to a 4-SPAD receiver fabricated in the same technology and introduced in 2020, the sensitivity is improved by 1.7 dB. The remaining gap to the quantum limit, which is at -73.7 dBm for 50 Mb/s, is reduced to 16.9 dB. A comparison to the state-of-the-art of SPAD receivers is included.**

Keywords – optical receiver; integrated optoelectronics; single-photon avalanche diode; high-voltage CMOS.

I. Introduction

Receivers with single-photon avalanche diodes (SPADs) are very interesting because of their very high gain [1], which eliminates the excess noise of avalanche photodiodes (APDs) in linear-mode [2]. A better sensitivity of SPAD receivers is therefore possible than for linear-mode APD receivers. Due to the very high gain of SPADs in the Geiger mode of larger 10^6, a digital output signal of the SPAD is possible and a digital gate (e. g. an inverter) can detect the absorption of a photon [3]. So, the excess noise of linear-mode APDs and electronic noise of an amplifier in a receiver is not relevant anymore.

However, SPADs are not ideal devices. Thermally generated charge carriers can trigger dark counts. During a Geiger mode event, traps can be filled and those can release charge carriers statistically with a certain time constant, which causes afterpulses. A long dead time and/or a fast active quenching of the SPADs have to be applied to reduce afterpulsing. So, there still can be Geiger mode events not caused by photon absorption. Already because of this non-ideal behavior of SPADs, one SPAD and absorption of one photon in a “1”-bit will not be sufficient to obtain a bit error ratio below 2×10^{-3}, which is needed to perform error correction [4]. Therefore, a kind of coincidence detection of at least two or more photons in a “1”-bit will be necessary.

If these issues can be handled, the final sensitivity is defined by the Poisson statistics of light sources like light emitting diodes and laser diodes, which causes the so-called quantum limit [5].

The first SPAD receiver containing 32×32 SPADs was designed for a high dynamic range and its sensitivity of −31.7 dBm at 100 Mbit/s and 450 nm wavelength [6], where the quantum limit is at −63.6 dBm, was quite moderate. A receiver with 100 SPADs was introduced for 20 Mbit/s in [7], but unfortunately no sensitivity was reported. We had investigated a 4-SPAD receiver following the simple idea that 4 SPADs with an afterpulsing probability of 10% each should result in a bit error ratio of 10^{-4}, assuming afterpulsing as the dominant effect [8]. This 4-SPAD receiver was fabricated in 0.35 µm PIN-photodiode CMOS technology. Later, we realized a 4-SPAD receiver [9] in the same 0.35 µm high-voltage CMOS technology as we use for the 9-SPAD receiver in this work.

In section II, the used SPAD and the receiver will be described. Section III reports the properties of the SPADs implemented in the 9-SPAD receiver. The receiver performance is introduced in section IV. In section V, the suggested 9-SPAD receiver is compared to the state of the art of SPAD receivers. Conclusions are drawn in section VI.

II. SPAD and Receiver

The SPAD presented in Fig. 1 does not need any process modification. It can be fabricated in the XH035 (0.35 µm) high-voltage CMOS process of XFAB using the standard ASIC procedure.

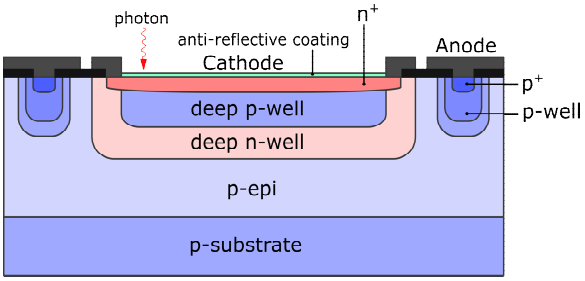

Fig. 1. Cross section of the integrated SPAD (not in scale).

The multiplication zone extends from the n+/deep-p-well junction into the deep p-well. The deep n-well compensates part of the deep p-well doping and part of the standard epitaxial layer doping. In such a way, this reachthrough avalanche photodiode allows for the depletion of the p-epi layer at an acceptable reverse voltage. The breakdown voltage of this SPAD is about 68 V [10], which is well within the isolation capabitlity of this process. So, this SPAD can be integrated together with transistors on the same chip. This SPAD was characterized in [11]. The photon detection probability (PDP) of the SPAD increases with the excess bias voltage. Thanks to the anti-reflection coating being available in the 0.35 µm high-voltage CMOS process used, the PDP for 635 nm and 6.6 V excess bias voltage is 45% [9].

The active quenching circuit described in detail in [12] was slightly improved. The principle of the quenching circuit is shown in Fig. 2. When the SPAD fires, the avalanche current increases and the voltage drop across R_C (actually realized as an active resistor MOSFET) grows. When the threshold V_{REF} is undercut, the comparator decides and the quenching switch is closed rapidly. To enable a large excess bias voltage of the SPAD of up to 6.6 V, the switches have to withstand this voltage. Therefore, the switches are realized as cascoded MOSFETs [12]. In such a way the fast 3.3 V transistors can be used although the excess bias of the SPADs can be up to 6.6 V. The closed quenching switch discharges the SPAD (slightly) below its breakdown voltage and the avalanche ends. After the dead time the quenching switch is opened and the reset switch is closed to charge the SPAD to the excess bias voltage again to make it sensitive for a new photon detection again. During the detection period, both switches are open. Via a bias input the dead time of the SPAD can be controlled in the range of 5.8 ns to 34 ns. It should be mentioned that the output pulses of the quencher have a shorter duration than the dead time [12].

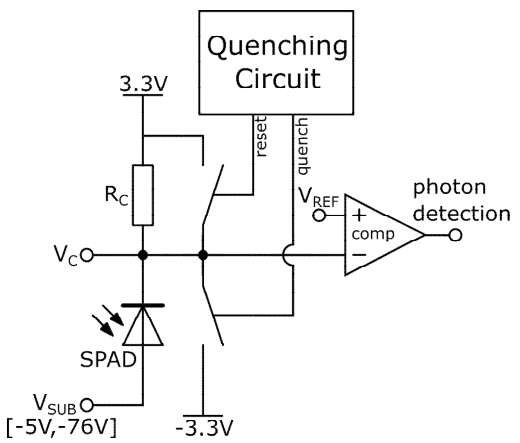

Fig. 2. Principle of the implemented active quenching circuit with comparator.

According to the supply voltages of -3.3 V and +3.3 V, which define the maximum excess bias of 6.6 V, the substrate potential of -71.3 V corresponds to a SPAD breakdown voltage of 68 V. If the excess bias of 4 V is desired, the substrate potential has to be set to -68.7 V.

In the presented 9-channel SPAD receiver, nine SPADs are equipped with one active quenching circuit each. The nine quencher outputs are connected to a bondpad each. The layout is introduced in Fig. 3 (upper part). The receiver chip was fabricated in 0.35 µm high-voltage CMOS (XH035) and the chip-photo is presented in Fig. 3 (bottom part). The size of this receiver chip is 2120 µm × 1640 µm. The diameter of the 9-segment SPAD detector is 490 µm and the optical fill factor is 49%. This large diameter was chosen because wide gaps between the concentric SPADs reduce the optical crosstalk. The concentrical segments were easier to layout than nine equal sectors or pieces of a tart. In addition, the distance between neighbouring pieces (especially closer to the center) would be too small concerning crosstalk. The SPAD segments are covered by an anti-reflection coating. The substrate contact ring surrounds the nine SPADs.

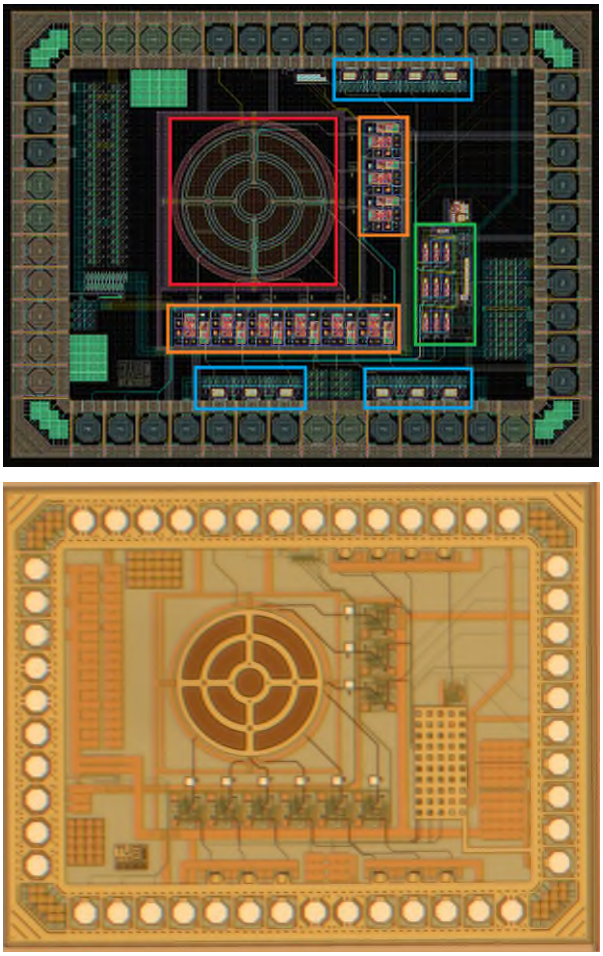

Fig. 3. Layout (top) and chip-photo (bottom) of receiver chip with 9 SPAD segments arranged in circular shape.

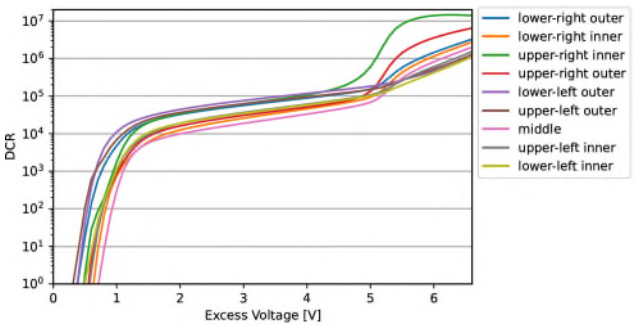

Fig. 4. Dark count rate of all 9 SPADs in the receiver.

I. Properties of SPADs

Since all nine quencher outputs are available, each SPAD could be characterized concerning dark count rate and afterpulsing probability. A measurement time of 100 s was used. The measured dark count rates (DCR) are presented in Fig. 4 in dependence on the excess bias voltage. The curves indicate that the SPADs can be operated for acceptable BERs of the receiver up to an excess bias of about 4.5 V.

The measured afterpulsing probabilities (APPs) of all 9 SPADs are shown in Fig. 5. The upper-right inner SPAD shows the worst APP as the worst DCR. Therefore, the highest possible excess bias voltage of 6.6 V cannot be used in the receiver.

Another source of digital noise in SPAD arrays is optical crosstalk. This effect happens because during impact ionization photons are emitted. These photons can be detected in other SPADs and trigger avalanche effects there although no “true” or “signal” photons fell into these SPADs. Optical crosstalk in a SPAD receiver increases the bit error ratio [13]. Therefore, the circular 9-segment SPAD detector was also characterized with respect to its optical crosstalk probability (OCTP). Figure 6 shows the total OCTP, i. e. between all of the nine SPADs. The total OCTP is below about 20% in the excess bias range relevant for the BER measurements presented.

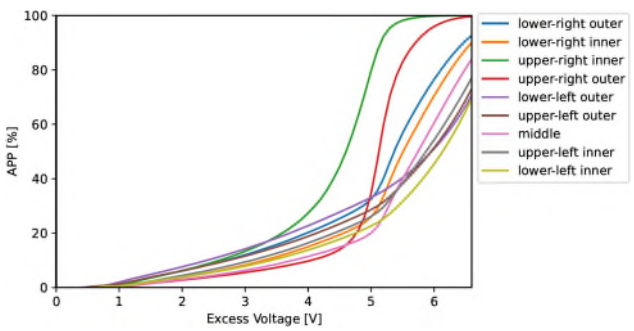

Fig. 5. Afterpulsing probability of all 9 SPADs in the receiver.

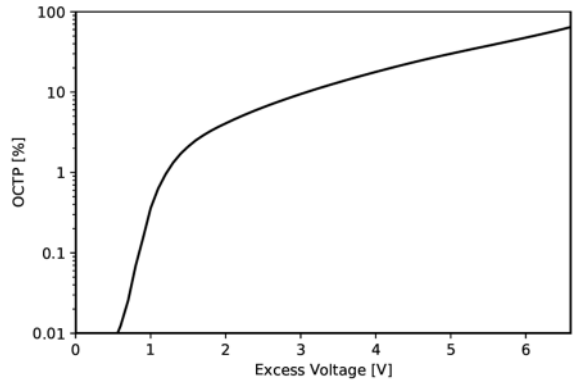

Fig. 6. Total crosstalk probability within the 9 SPADs of the receiver.

When having the large diameter of the 9-segment SPAD array in mind, the DCR, APP and OCTP seem to be reasonably low.

II. Receiver Performance

As light source for the receiver experiments a high-extinction-ratio direct modulated laser diode with a wavelength of 680 nm was used. The receiver was placed inside a dark box and an optical fiber fed by the laser diode was adjusted to the center of the 9-segment SPAD array. The height of the fiber end over the reciver was set that a minimum BER was obtained. The optical power was measured with a Thorlabs PM200 power meter and the chip was held at constant temperature with a Thorlabs TC200C TEC controller.

The measurements were done via LabView. The program ran on an NI PXIe-8840 controller. The 9 outputs of the quenchers were connected via an interface board to a NI-6589 I/O module. A NI PXIe-7972R FlexRIO FPGA generated the 50 Mb/s return-to-zero (RZ) PRBS7 signal to modulate the laser source. The RZ signal had a duty ratio of 50%. Two source measure units (NI PXIe-4132 and NI PXI3-4145) delivered the substrate voltage (anode voltage of the SPADs), the supply voltages, the control voltage for the dead time and V_{REF} for the comparators to the SPAD receiver chip. The FPGA processed the 9 data streams of the SPAD receiver according to the principles of a latched and non-latched method (see Fig. 7). The latched method implies that a photon detection after the dead time but within the same bit is not taken into account. Whereas a photon detection after the dead time is considered with the non-latched method. The threshold of photon counts within each bit could be set in the range of 1 to 9 The obtained bits were compared by the FPGA with the PRBS stream used for laser modulation. In this way, the bit errors were determined efficiently directly within the FPGA. The dead time was optimized for minimum BER. The best performance was obtained with dead times of somewhat less than 10 ns. The measurement time was 1s.

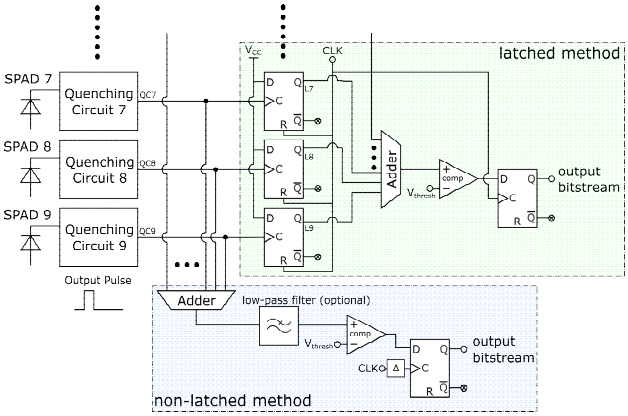

Fig. 7. SPAD receiver with 9 detectors, quenching circuits and postprocessing realized in an FPGA with a latched and non-latched method. The digital adder counts photons with equal weights.

Figure 8 shows the obtained BERs at 50 Mb/s for the non-latched processing for different thresholds in dependence on the average optical power. The sensitivity of the receiver is best for the thresholds of 2 and 3. The sensitivity for the threshold of 2 is -56.81 dBm for the non-latched processing method.

Figure 9 presents the BERs at 50 Mb/s for the latched processing for all thresholds that reached the BER limit of 2×10^{-3} for error correction. The best thresholds are 3 and 4 photon counts in a "1" bit. The sensitivity for the threshold of 3 is -56.26 dBm for the latched processing method. We can conclude that the non-latched processing method is better appropriate for determining the receiver sensitivity.

For the curves in Figs. 8 and 9, the substrate voltage (anode) voltage of the SPADs, i. e. the excess bias voltage, was held constant at the values for which the BER of 2×10^{-3} was achieved at the lowest optical power. The BER could be reduced (see Figs. 10 and 11), when the optimum substrate voltage, i. e. the optimum excess bias voltage, was used for each optical power.

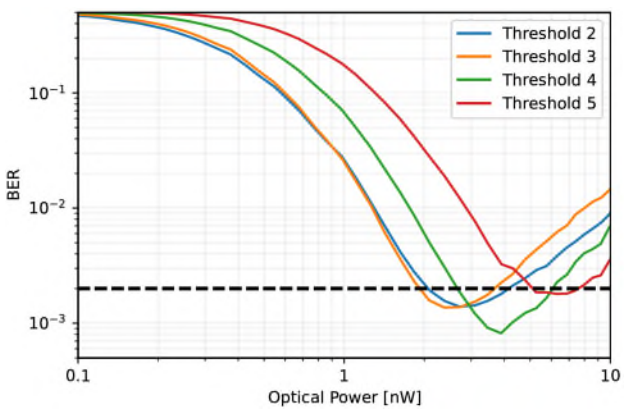

Fig. 8. Bit error ratio for the non-latched processing.

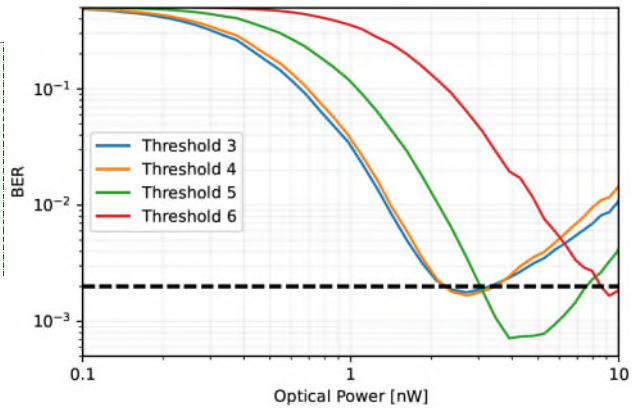

Fig. 9. Bit error ratio for the latched processing.

With this additional degree of freedom, the minimum BER of 10^{-4} is achieved at about 9 nW optical power with a threshold of three photon detections in the case of the non-latched processing. With latched processing the minimum BER of 2×10^{-4} is present for about 7 nW optical power with the threshold of four photon counts. The excess bias voltages for BER<2×10^{-3} are lower than about 4 V for both cases (non-latched and latched processing). For higher excess bias voltages the bit errors increase because of rising DCR, APP and OCTP.

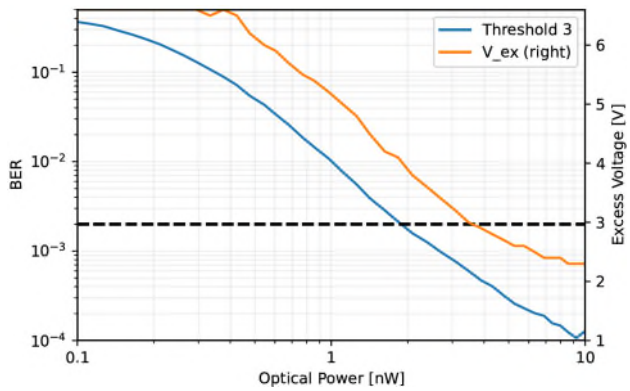

Fig. 10. Bit error ratio for the threshold of 3 photons (left) and excess bias voltage (right) for the non-latched processing.

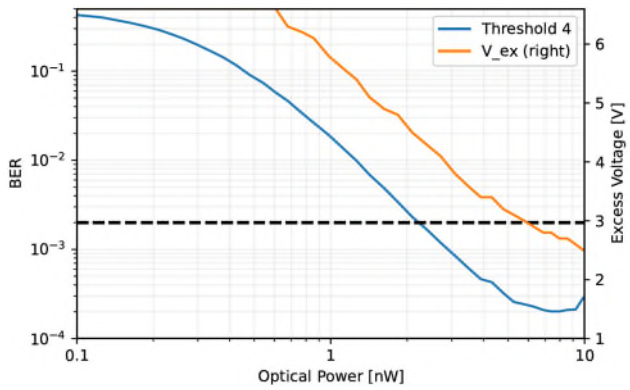

Fig. 11. Bit error ratio for the threshold of 4 photons (left) and excess bias voltage (right) for the latched processing.

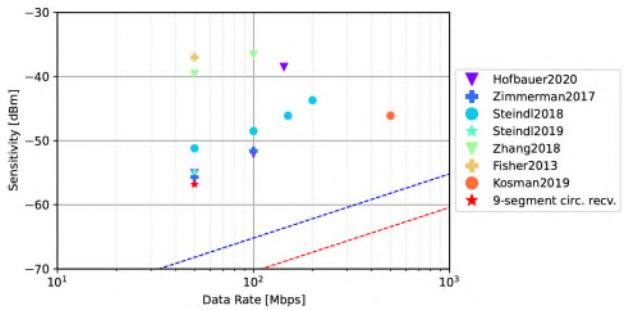

Fig. 12. Comparison of the sensitivity to the state of the art with quantum limits for BER=2×10^{-3} (blue line) and for BER=10^{-9} (red line).

I. Comparison

The 9-SPAD receiver (represented by the red star in Fig. 12) improves the sensitivity compared to a 4-SPAD receiver [9] (-55.1 dBm, represented by the violet triangle in Fig. 12) in the same 0.35 µm high-voltage CMOS technology at 50 Mb/s by 1.7 dB, which corresponds to a reduction of the necessary optical power for BER=2×10^{-3} by about 30%. The reason for this is that still a few SPADs from the 9 SPADs can detect photons if some are already dead after detection in the same bit. Therefore, less optical power is sufficient compared to the 4-SPAD receiver.

Compared to the 4-SPAD receiver in 0.35 µm PIN-photodiode CMOS [8] (represented in Fig. 12 by the blue +) with a sensitivity of -55.7 dBm at 50 Mb/s, the 9-SPAD receiver shows an improvement in sensitivity of 1.1 dB.

The 4-SPAD receiver of [14] (represented by the blue circle in Fig. 12) in 0.35 µm PIN-photodiode CMOS technology has a sensitivity of -51.2 dBm at 50 Mb/s. Another 4-SPAD receiver in 0.35 µm CMOS achieved a sensitivity of -54.9 dBm [15] (see the blue star in Fig. 12).

A receiver in 0.18 µm CMOS containing 60 SPADs achieved a sensitivity of -39.6 dBm at 50 Mb/s [16] (represented by the green triangle in Fig. 12). This sensitivity was mainly due to the low optical fill factor of 3.2%.

A 64×64 SPAD receiver in 0.13 µm CMOS showed a sensitivity of -41.6 dBm at 500 Mb/s [17]. This data point is the orange circle in Fig. 12.

II. Conclusion

There were several attempts to develop SPAD receivers reducing the gap to the quantum limit. Increasing the number of SPADs in a receiver improves the sensitivity and enables higher data rates. The receiver circuit and system complexity increase in turn. But dark counts, afterpulsing, optical crosstalk and the dead time prohibit to reach the quantum limit. The photon protection probability has to be increased to approach the quantum limit closer – however without increasing the dark count rate, afterpulsing probability and optical crosstalk. Finally, these issues will require higher purity in CMOS processing. We should, however, be aware that silicon technology and wafer fabrication are already at a very high level.

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