Bulk-Driven Fully Differential Difference Amplifier for Ultra-Low Voltage Applications

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Abstract—This paper deals with the design and analysis of a fully differential difference amplifier (FDDA) based on a pseudo differential topology that was implemented in a 130 nm CMOS technology. The proposed FDDA can reliably work with its power supply voltage as low as 0.4 V. The FDDA was designed using the bulk-driven technique, and Rail-to-Rail (RtR) input voltage range was ensured through the use of bulk-driven input transistors. Additionally, the RtR input/output CMFB, based on FDDA topology, was proposed. The output voltage range is near RtR (±0.36 V). The CMRR and PSRR of 60.2 dB and 64.4 dB was achieved, respectively. The proposed FDDA shows very good linearity in wide output range, thus the THD of -156 dB@1 mV was reached. Furthermore, the proposed FDDA was used as a building block of an ultra-low voltage-to-frequency converter.

I. INTRODUCTION

Recent trends towards ultra-low voltage (ULV) integrated circuits (ICs) design are backed by modern nanoscale CMOS technologies, where the supply voltage is continually scaled down. In this way, demand for long-life and portable electronics can be satisfied by increasing the battery life. The ultra-low value of the supply voltage also reduces the overall power consumption of digital ICs, since it is proportional to the square of the supply voltage value. On the other hand, the power consumption of analog ICs does not decrease by scaling down the supply voltage, since the consumption depends on the required signal-to-noise ratio (SNR). Additionally, the reduction of supply voltage can decrease the dynamic range (DR) of analog ICs, since it directly depends on the supply voltage value. For these reasons, new design techniques and novel topologies of analog ICs for ultra-low supply voltage have to be developed.

In this paper, the design of a ULV bulk-driven FDDA, based on a pseudo-differential topology, is presented and its main parameters are analyzed. In Section II, backgrounds of the FDDA and common-mode feedback (CMFB) circuits are presented. The proposed FDDA, as well as other used sub-circuits (Common-Mode Feedforward (CMFF) and CMFB), are described in Section III. The achieved results are presented in Section IV. In Section V, an application of the proposed FDDA, a ULV voltage-to-frequency converter, is shown. In the last section, the obtained results are discussed.

II. BACKGROUND

A. Fully Differential Difference Amplifier

To increase the DR of ULV analog ICs, fully differential (FD) signal processing has to be employed. Besides, the FD approach can improve the noise immunity as well as the power supply rejection (PSRR) of analog ICs. One of very advantageous building blocks used in the FD signal processing approach is a fully differential difference amplifier [1]–[3]. The most important advantage of the FDDA is high common-mode signal rejection [3]. Furthermore, the FDDA allows realization of both the non-inverting and inverting amplifiers without using resistors in the signal path and therefore, it can be efficiently used in low-noise applications.

In the case of ULV applications, where the supply voltage is usually less than 1 V, the possibility of using standard amplifier topologies is rather limited. Standard differential amplifier topologies are usually based on conventional structures [3] composed of four or more stacked transistors. Thus, these topologies require quite high supply voltage values. Therefore, dedicated low-voltage design techniques have to be employed. In order to achieve low-voltage operation, the bulk-driven technique was used in [4]–[7]. Nevertheless, in [4], [5], [7] the supply voltage is about 1 V. In [6], the bulk-driven quasi-floating gate technique was used, decreasing the supply voltage to 0.5 V. In all of these cases, the amplifier topology was based on the conventional differential structure. Another possibility to decrease the required supply voltage of the amplifier is to use the pseudo-differential difference (PDD) topology. This topology employs a differential pair without a tail source, which represents two independent common-source amplifiers. Additionally, the PDD topology can effectively increase the input and output voltage ranges. On the other hand, disadvantages of the PDD include high sensitivity to process, voltage and temperature variations (PVT) as well as a low value of the CMRR parameter, due to the absence of the tail source. Therefore, a CMFB or CMFF circuit is usually employed to stabilize the operational point and to increase the CMRR of the PDD amplifier [8], [9].

The general block diagram of a FDDA is shown in Fig. 1, where one can observe that the FDDA has two differential inputs that convert two differential voltages into currents. Then, these currents are subtracted from each other and...
converted back into a differential voltage, which is amplified using the differential output stage. The differential output voltage of the FDDA can be expressed as:

\[ V_{OUT} = A[(V_{+IN} - V_{-IN}) - (V_{+IN2} - V_{-IN2})], \]  

(1)

where \( V_{OUT} = V_{+OUT1} - V_{-OUT2} \) is the differential output voltage, \( V_{+OUT1} \) and \( V_{-OUT2} \) are the single ended output voltages, \( A \) is the total gain of the FDDA, while \( V_{+IN} - V_{-IN} \) and \( V_{+IN2} - V_{-IN2} \) are the first and second input differential voltages, respectively.

B. Common-Mode Feedback Circuit

In the case of a PDD amplifier, design of a high gain CMFB belongs to the crucial issues, especially from two points of view: 1) The missing tail current radically degrades CMRR and PSSR well below 100 dB [10], and according to [11], improving the gain of the CMFB can significantly suppress this effect. However, we must note that the overall impact of the CMFB mainly depends on the main amplifier performance itself (gain, mismatch, etc.) [12]. High values of these parameters tend to be more challenging to achieve using the bulk-driven approach. 2) Ensuring high common–mode (CM) loop gain under all PVT conditions can radically reduce permanent regulation deviations, that may be noticeable in ULV applications [13]. To be able to cope with these phenomena, two main approach categories exist, e.i. switched-capacitor (SC–CMFB) and continuous time (CT–CMFB) realizations. In general, a capacitor based CMFB such as SC–CMFB or its continuous-time counterpart (CTC–CMFB) from [14] do not resistively load the main amplifier output, do not cause extra power dissipation (except for the switching loss in SC–CMFB based topology) and have no headroom requirements, meaning that rail-to-rail (RtR) output swing of the main amplifier can be achieved [14], [15]. In contrast, using of SC–CMFB is usually restricted to time-discrete circuits, where the phenomena like clock feedthrough noise, charge injection problems and high switching frequency requirements \( (f_{SW} > GBW) \) must be taken into account [14]–[16]. Additionally, direct implementation of SC–CMFB under ULV conditions is restricted by the switching transistors not being able to turn on fully, due to the limited overdrive voltage. The CTC–CMFB behaves only as a CM detector (balanced capacitive CM–sense network) without native gain [14], [17], and therefore is not suitable for use in PDD amplifiers, where extra high gain is the priority requirement for the CMFB.

The most common implementation of a CT–CMFB for both high and low voltage applications is the resistor averaging circuit (balanced resistive CM–sense network), which performs only as a detector, and therefore requires an additional error amplifier with high gain (similar to the capacitor-based CMFB). The common characteristics of the CT–CMFB include high linearity, high immunity to the differential signal and a wide voltage swing, without a significant offset of the common-mode voltage compared to a differential difference amplifier (DDA) based CT–CMFB implementation. However, sensing resistors should be very large to guarantee that the gain of the system is not deteriorated by, leading to considerable noise and parasitic effects [13], [16], [17]. For this reason, a buffered approach has been part of many designs, to avoid the resistive loading while reducing the circuit area by using smaller resistors. The easiest way of implementing this method is a follower-based realization that is, in general, not implementable for ULV applications, due to voltage headroom requirements [18] (however, the input range can be improved by utilizing a bulk-driven topology [18]) similar to a CT–CMFB employing transistors in the deep triode region as sensing elements [16]. On the other hand, an extended solution based on an auxiliary complementary sensing method drawn from the differential pair topology, eliminating the minimum output voltage, can be a promising candidate [16].

The before mentioned approaches mostly utilize passive devices to form the CM detector, with gain of a few dB at best, followed by an error amplifier to achieve additional gain enhancement. A DDA [10], [11], [13], [18]–[22] may be able to combine both functionalities into a single block, like a pseudo-differential CM amplifier (PDCM), which represents a suitable solution for ULV designs due to only a two–above transistor topology [10], [15]. The PDCM structure can be applied to the PDDA configuration [10] or transformed from parallel MOS active resistors [15]. Generally, the incorporation of the differential pairs with nonlinear behaviour causes linearity degradation and increases sensitivity to the differential signal, which is declared as the main problem of this approach [15], [18]. Good discussion on this topic can be found in [12]. For this reason, the mostly linear behaviour of the input differential transistor pairs with small aspect ratios \( (W/L) \) together with the cross–connection and current based CT–CMFB topology have been recommended in [12], and found their applications in several ULV designs [11], [13], [18], [20]–[22].

III. PROPOSED PSEUDO FULLY DIFFERENTIAL DIFFERENCE AMPLIFIER

A. Pseudo FDDA topology

The schematic diagram of the proposed ULV pseudo FDDA (PFDDA) circuit is depicted in Fig. 2. The PFDDA was designed in a 130 nm CMOS technology and can reliably operate at the supply voltage of 0.4 V. The first stage of the proposed topology is based on the cascode PFDDA, while the second stage is a conventional
common-source amplifier. The input bulk-driven transistors M1-M4 are used to obtain the rail-to-rail input voltage range, and together with transistors M5-M8, represent a cascode topology. However, bulk transconductance of a MOS transistor is given by $g_{mb} \approx 0.2 g_{in}$, which means that the gain and gain-bandwidth product (GBW) of the proposed PFDDA will be decreased. Transistors M9 and M10 are used as the active load in order to achieve the current-to-voltage conversion. The simple common-source amplifier (M11-M14) was used as the second stage of the proposed PFDDA. To decrease the threshold voltage of transistors M11-M14, the bulk terminals of NMOS and PMOS devices are connected to the supply voltage ($V_{DD}$) and ground, respectively. This is possible to fabricate since the proposed PFDDA was designed in 130 nm twin-well CMOS technology which offers isolated bulk terminals for both NMOS and PMOS transistors.

B. Proposed CMFF circuit

The pseudo differential topology is sensitive to a difference between the common-mode voltages at the inputs. For this reason, a CMFF circuit was employed in order to regulate the gate bias voltage of the input transistors M1-M4. The developed CMFF circuit is shown in Fig. 2. Since the PFDDA has four inputs, two CMFF circuits were used. Transistors M17-M20 follow the input signal of the PFDDA, while diode-connected transistors M21-M22 convert the current generated by them to a (bias) voltage that is proportional to the common-mode voltage at the PFDDA inputs. In the case of a purely differential input signal, there is no change in the current flowing through the diode-connected transistors M21-M22, and the voltages at the CMFF output (voltage drops on diode-connected transistor M21 and M22) is stable. However, in the case of a difference between the values of the common-mode voltage at the PFDDA inputs, the current through transistor M21-M22, and the resulting voltage drop, will be changed. This principle was used to regulate the gate voltage of the input transistors M1-M4, when the common-mode voltage at the inputs is changed, and causes less PFDDA sensitivity to the common-mode voltage as well as process and temperature variations.

C. Proposed CMFB circuit

A rail-to-rail input/output, current steering (high impedance current-mode systems), 3-stage CT–CMFB with the first stage based on the FDDA topology has been proposed (Fig. 3b). The proposed CT–CMFB modifies the robust, low differential signal sensitivity topology published in [15], where the output diode $MTA$ was replaced by transistors $M_{2x}$–$M_{3x}$, with a voltage reference connected to their bulk electrodes. The complementary topology has not been implemented into our design because the auxiliary current source $M_{1x}$ is sufficient to keep DM–CM conversion of the first stage reasonably low as demonstrated in [13], [22]. The RR input and output ranges are ensured by the bulk–driven technique and push–pull differential-to-single ended stage, respectively.

\[
A_{cmfb, st} = \frac{V_{DM, cmfb}}{V_{CM, cmfb}} = \begin{cases} 
\frac{g_{m3} \| r_{ds3}}{2} & \text{for} \ M_{2x}, M_{3x} \\
g_{m3} r_{ds3} & \text{for} \ M_{1x}
\end{cases} \quad \text{(Fig. 3a)}
\]

According to [12], [18], the CM loop gain of the CMFB should be at least equal to the external DM close loop gain of the amplifier. The same assertion is also valid for loop gain-bandwidth products [12]. In other words, the performance of both loops should be comparable. In ULV applications, this requirement increases demand for high currents leading to larger power consumption and circuit area. For these reasons, the 3-stage CT–CMFB has been employed to keep the idea of moderate inversion design while achieving the necessary gain. To profit from the differential structure, the first stage has been designed in this manner (similar to designs shown in Fig. 3a [11]), which is based on independent positive and negative P–type CT–CMFB circuits (Fig. 3b). In the proposed CT–CMFB, high gain is achieved by the CMFB–FDDA configuration with high output impedance. The resultant gain can be described by Eq. 2b) (under the following presumption $M_{2x} = M_{3x}$ and $M_{5x} = M_{6x}$). This is the main difference when compared to popular diode-connected loading configuration [15], [18], which are intentionally expanded by a partially cross–coupled positive feedback [11], [20] or a local feedback, in order to improved the dynamic current [21].
Eq. 2 shows that comparable gains can be achieved (because of the multi-stage design, and it has been solved by Miller compensation capacitors and additional $Gm - C$ stage in both CMFBs.

we look closer at the only similar solution presented in [11], the solution proposed in this paper, exhibits more symmetrical behaviour with the extensive linear range of single ended outputs $OUT_X$ compared to its competitor, which is directly reflected into the differential outputs as the tradeoff between gain and the operation range (Fig. 4). Finally, by the avoiding the partial feedback implementation, designs rather robust to PVT variations can be achieved. We must note that the stabilization issue is very challenging in the multi-stage design, and it has been solved by Miller compensation capacitors and additional $Gm - C$ stage in both CMFBs.

PFDDA can operate in near to rail-to-rail output voltage range. The worst case (from the output range point of view) can be observed in the fast-fast (FF) corner at temperature of $85^\circ C$, where the output range of $\pm 0.36$ V was achieved. The deviation of the maximum output voltage is $24$ mV when all the process corners and the whole temperature range were considered.

In order to investigate the linearity of the proposed PFDDA, the closed-loop DC transfer characteristic was obtained (Fig. 6). The PFDDA was simulated in the voltage buffer $(AV = 1)$ configuration. If we consider all process corners and the whole temperature range, the output voltage range of the PFDDA will be about $\pm 0.3$ V in the worst case (FF, $85^\circ C$). However, the PFDDA can operate in the rail-to-rail input and output voltage ranges, but with reduced linearity.

In order to obtain the dependence of the linearity on the input voltage amplitude, the total harmonic distortion (THD) in the open-loop (OL) and closed-loop (CL) configurations of the PFDDA has been investigated. The dependence of the THD parameter on the differential input voltage amplitude is shown in Fig. 7. In the worst case, for the input amplitude of $1$ mV, the THD parameter reaches the value of $-13.9$ dB and $-150.8$ dB in OL and CL configurations, respectively. Nevertheless, THD is less than $-20$ dB for all values of the input voltage amplitude below $300$ mV in the CL configuration.

Fig. 8 shows the frequency response of the PFDDA, where all process corners were taken into account. In the typical case, the low-frequency gain of the PFDDA is $64.24$ dB and the
Gain-bandwidth of 2.4 MHz was achieved. It can be observed that in the worst case, which corresponds to FF corner and temperature of 85°C, the low-frequency gain is about 50 dB and GBW parameter reaches value of 6.17 MHz. On the other hand, in the case of slow-slow (SS) corner and temperature of –20°C, gain of the proposed PFDDA is about 70 dB but the GBW will be decreased to the value of 483 kHz. These parameters were obtained for the load capacitance of 10 pF.

The main parameters of the proposed PFDDA are summarized in Table I, where all process corners and the temperature range from –20°C to 85°C are considered.

### Table I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_v$ [dB]</td>
<td>$C_L = 10 \text{ pF}$</td>
<td>50.3</td>
<td>64.24</td>
<td>69.8</td>
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<tr>
<td>GBW [Hz]</td>
<td>$C_L = 10 \text{ pF}$</td>
<td>483kHz</td>
<td>2.43M</td>
<td>6.17M</td>
</tr>
<tr>
<td>BW [Hz]</td>
<td>$C_L = 10 \text{ pF}$</td>
<td>1kHz</td>
<td>6.45kHz</td>
<td>46.7kHz</td>
</tr>
<tr>
<td>CMRR [dB]</td>
<td>$V_{DD} = 0.4 \text{ V}$</td>
<td>40</td>
<td>60.2</td>
<td>100</td>
</tr>
<tr>
<td>PSRR [dB]</td>
<td>$V_{DD} = 0.4 \text{ V}$</td>
<td>20</td>
<td>64.4</td>
<td>120</td>
</tr>
<tr>
<td>THD [dB]</td>
<td>$V_{in,lin} = 1 \text{ mV}$</td>
<td>–156</td>
<td>–150</td>
<td>150</td>
</tr>
<tr>
<td>SR [V/µs]</td>
<td>$V_{in,pulse} = 200 \text{ mV}$</td>
<td>0.55</td>
<td>2.95</td>
<td>6.1</td>
</tr>
<tr>
<td>Output voltage range [V]</td>
<td>$V_{DD} = 10 \text{ pF}$</td>
<td>–0.36</td>
<td>–0.36</td>
<td>0.36</td>
</tr>
<tr>
<td>Total power [µW]</td>
<td>$V_{DD} = 0.4 \text{ V}$</td>
<td>8.7</td>
<td>78.4</td>
<td>385.3</td>
</tr>
</tbody>
</table>

### V. APPLICATION OF THE PROPOSED PFDDA

The performed analysis has shown that the proposed PFDDA has very good linearity in a wide output voltage range. Additionally, the use of bulk-driven input transistors ensures the rail-to-rail input voltage range. The presented PFDDA represents an universal building block that can be used...
in low-voltage differential systems. The developed PFDDA was used as a building block of a voltage-to-frequency converter (VFC). The block diagram of the converter is shown in Fig. 11. It can be observed that the PFDDA was employed in the closed-loop configuration as an amplifier and voltage-to-current converter. This implementation will be used for on-chip measurement of current consumption.

![Fig. 11. Application of the PFDDA in a voltage-to-frequency converter](image1)

The voltage-to-frequency dependence is shown in Fig. 12. The sensitivity of the first and the second output is 161 Hz/mV and -244 Hz/mV, respectively.

![Fig. 12. VFC transfer characteristics](image2)

VI. CONCLUSION

The novel low-voltage FDDA circuit, based on the PDDA topology and designed in 130 nm CMOS technology, was presented. As demonstrated, the designed PFDDA represents a building block for low-voltage applications, where the supply voltage of less than 0.4 V, differential signal processing as well as high dynamic range and low distortion are required. The proposed PFDDA was used as a building block of a low-voltage voltage-to-frequency converter in order to increase its dynamic range.

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