Uninterruptible Power Supply System for Railway Infrastructure with Power Factor Correction and Immunity to Energy Strike

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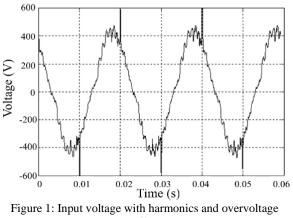
Abstract— This article deals with an uninterruptible power supply (UPS) for infrastructure equipment used in the railway system. The main feature of this UPS is the high power factor and resistance to overvoltages that occur in the railway network. Power factor correction (PFC) is done by adding a boost DC converter. The resistance to overvoltages is achieved by means of protective elements, i.e. varistors and inductors, as well as an additional overvoltage detection in the power supply network. Based on the output of the mentioned device, the part of the topology intended for power factor correction can be switched off.

Keywords – Uninterrupted Power Supply (UPS), Power Factor Correction (PFC), overvoltage protection, railway power supply system

I. INTRODUCTION

The importance of rail transport is extremely significant, and rail transport based on electric traction is particularly important. The traction vehicles are mainly supplied by a 25 kV, 50 Hz catenary [1], while the signal, safety, and security systems are supplied by the same line through a transformer and a uninterrupted power supply (UPS) with direct and/or alternating voltage (230 V, 50 Hz; 3 x 400/230 V, 50 Hz; 3 x 380 V, 83,33 Hz; 12 V_{dc}; 24 V_{dc}; 110 V_{dc}) [2]. The UPS usually consists of a rectifier in the input stage, a DC / DC link consisting of capacitors to reduce voltage ripple, and a DC / DC or DC / AC converter at the output [6]. In addition to noise immunity, an important requirement for UPS systems used to supply infrastructure equipment is a built-in power factor correction (PFC) in the input stage, i.e., compliance with power quality regulations such as IEC 61000-3-2 and IEEE 519 [3], [4]. Its main task is to reduce total harmonic distortion (THD) and electromagnetic interference (EMI).

Although the voltages of the power supply grid are strictly standardized, there are sections of the grid where high-voltage disturbances occur when a train passes through, causing damage to low voltage equipment supplied from the same grid. Disturbances present in the power supply network of the railway system, as shown in Figure 1, caused by the passing thyristor locomotive, disrupt proper operation and may even destroy the gridconnected UPS -es [2][5]. This article analyzes a UPS that has a high degree of immunity to interference. The effectiveness of protective components against overvoltage is considered. In addition, the UPS structure is upgraded with a circuit for power factor and THD correction [7], as well as with a sensor for overvoltage detection.



spikes

After the introduction, the 2nd chapter of the article discusses the structure of the UPS with varistors and inductors as protective elements. The chapter describes the model and parameters of the UPS, as well as its operation. In Chapter III, a simulation model was created, and simulation results of the output voltage caused by the input voltage with multiple higher harmonics and overvoltages are presented. The model of UPS with the voltage disturbance sensor and the PFC circuit is analyzed in Chapter IV. The simulation results show the behavior of the system and the improvement caused by the mentioned circuits. Concluding remarks are made in Chapter V, and then the list of references follows.

II. UPS STRUCTURE

The structure of the considered UPS is shown in Figure 2. The UPS is fed from the low-voltage side of the transformer, whose high-voltage side is connected to the power supply network of the railroad network (25 kV). This implies that all disturbances that occur on the high-voltage side of the transformer are reflected to the low-voltage side via an inductive link. These disturbances include higher harmonics, overvoltages and voltage spikes.

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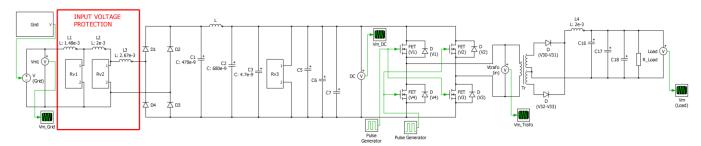


Figure 2: Model of UPS structure

A. AC distribution and rectifier stage

To reduce the harmful effects of overvoltages on the operation of UPS in the input part of the AC distribution, a protection consisting of inductors and varistors (L1, L2, Rv1, Rv2) is used. The varistors are from the manufacturer Epcos, types: VDR B40K320 and VDR B40K275. An example of such a varistor model and its response is shown in Figure 3. Several rectifier stages connected in parallel are connected to this input section of UPS (one such stage is shown in Figure 2). The rectifier stage was implemented with a single-phase diode bridge circuit. Between each rectifier stage and the input AC distribution there is an inductance which serves to reduce the charging current of the capacitors forming the DC link in case of an overvoltage. The inductance is L3=2.67 mH. The DC intermediate circuit consists of three capacitors connected in parallel, each with a capacitance of 2.470 µF. This part of the UPS also contains components that serve as EMI filter and another Epcos varistor, model S20K300 (Rv3). The EMI filter is implemented by connecting capacitors and inductor (C1, C2, C3, L), where the inductor L is essentially common mode inductor.

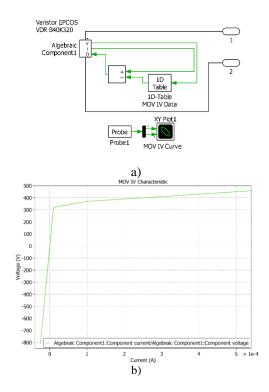


Figure 3: Varistor: a) model, b) UI characteristic

B. Full-bridge DC/DC converter

The full bridge DC /DC converter is connected after the DC link, (C5, C6, C7). The task of this stage of the UPS is to control the level of the output DC voltage and the galvanic isolation. On the primary side of the high-frequency transformer is a single-phase bridge circuit consisting of hybrid current-bidirectional switches. The switches are implemented by MOSFET and body diode. On the secondary (low voltage) side of the transformer midpoint connection. The additional low-pass filter is connected between the output of the rectifier and the load (battery). The switches on the primary side of the transformer are controlled to produce the three-level voltage.

III. UPS WITHOUT POWER FACTOR CORRECTION

A. Model and model parameters

The UPS model described in this chapter is based on a well-known commercial solution, (Figure 2), which will be extended in later stages of the article to include the input voltage disturbance sensor and PFC with the corresponding control algorithm. At this stage of the article, the model doesn't include any sensor and neither additional protection in this regard. The most relevant parameters of this model are listed in Table 1.

TABLE 1: PAF	AMETERS OF THE	EXISTING MODEL
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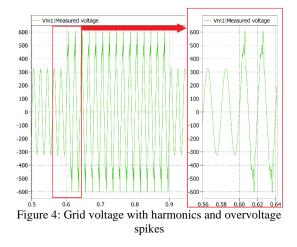
Macromodel /	Element	Parameter	Value
Function			
AC distribution	L1	Inductance	1.48 mH
and input	L2	Inductance	2 mH
protection	Rv1	U-I char.	do 320 V
circuit	Rv2	U-I char.	do 275 V
	Rv3	U-I char.	do 300 V
Rectifier	D1 - D4	Fwd. voltage	1 V
		Ron	10 mΩ
Input EMI filter	C1	Capacitance	470 nF
	C2	Capacitance	680 nF
	C3	Capacitance	4,7 nF
	L	Inductance	1.13 mH
Intermediate	C5 - C7	Capacitance	2x470 μF
DC circuit			
Bridge connection	FET	Ron	10 mΩ
connection	D	Fwd. voltage	0.7 V
		Ron	1 mΩ

The appearance of higher harmonics, overvoltages and other disturbances in the railway transport system is well known. The power supply V(Grid) at the input UPS is directly connected to the block/macro model Grid, where the actual model of the grid is located. The macro model consists of a combination of base sine wave $230\sqrt{2} V, 50 Hz$, superimposed by odd harmonics (up to and including the 17th harmonic), overvoltage of about 140 V, and low signal noise with random characteristics. By superimposing these disturbances on the network voltage with a sinusoidal waveform, the actual waveform of the voltage on the dedicated line of the double-track railway is simulated, Figure 4.

In order to preserve the proper operation of the existing UPS and protect the output voltage of the effects of the higher harmonics and overvoltage on the voltage waveform, two inductors (L1 and L2) and two varistors (Rv1 and Rv2) are used in the AC distribution and protection part. The main task of this protection is to try to eliminate (over)voltage spikes and, if possible, higher harmonics with significant amplitudes. In practice, other solutions such as surge arresters are also used, but recent research suggests that solutions from the field of power electronics may be helpful [8]. Between the AC distribution and protection on one side and the rectifier bridge on the other, inductor L3 is placed. Its function is to further reduce the voltage rise. The effect of these protection elements was tested in further simulations.

B. Simulation experiment

The objective of these simulation experiments is to confirm the effectiveness of the previously described protection elements with the input voltage shown in Figure 4. The disturbances present in the input voltage in the form of higher harmonics and overvoltages are active in the time span of 300 ms (between 600 - 900 ms). This form of input voltage occurs on the power line of one track of a double-track railway at the moment when the locomotive passes by the traction power substation. UPS operation with and without protection is simulated and the obtained results are compared. The waveforms to be considered are: (i) voltage stress of the diodes in the bridge circuit (reverse voltage), (ii) voltage of the DC link, (iii) voltage stress on the transistors in the bridge circuit, (iv) voltage at the transformer, and (v) load voltage.



A comparison of these waveforms with and without protection is shown in the following figures. The effect of the protection can be seen in the reverse voltage of the diode in the rectifier bridge circuit, Figure 5. With the input protection, the voltage load is significantly lower (510 V on average compared to 556 V without protection).

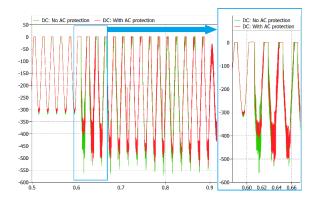
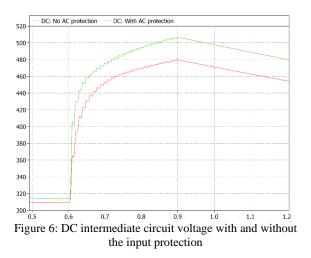


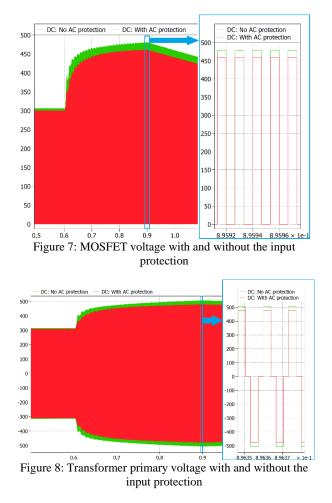
Figure 5: Reverse voltage of the diode in the rectifier bridge with and without the input protection



The results of the simulation of the DC link voltage with and without protection included are presented and shown in Figure 6. In the steady state, which occurs within the first 600 ms, a sinusoidal voltage appears at the input, after which higher harmonics, overvoltages and voltage spikes occur. The disturbances in the grid voltage cause significant increase of the DC link voltage. After 900 ms, the voltage of the DC link slowly decreases. When the protection is not used, the voltage of the DC link increases to 482 V, which is higher than the voltage of 461 V when the protection is used. After the locomotive passes TPSS, the influence of the higher harmonics slowly decreases, but the return to the stable voltage with the protection not used requires a longer time (1500 ms).

Similar to the previous considerations, the effect of voltage disturbances, but also the effect of protection, can be seen in the voltage waveforms of transistors with body diodes connected in a bridge circuit, Figure 7.

Figure 8 shows the voltage waveforms on the primary side (high voltage side) of the DC /DC converter transformer. When the protection is used in the presence of higher harmonics and voltage spikes in the input voltage, the change in the DC link voltage is minor (the maximum voltage here reaches 482 V).



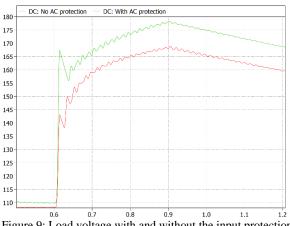


Figure 9: Load voltage with and without the input protection

Figure 9 shows voltage waveforms on the load side. The analysis of the simulation results presented earlier leads to the conclusion that the protection consisting of inductors and varistors in the input circuit of the UPS (described in chapter III, table 1) educes the voltage stress on the components of the UPS caused by overvoltages and higher harmonics occurring in the input voltage due to the passage of the thyristor locomotive. However, the question arises as to how effective this protection is when a PFC subsystem is included in the UPS in form of a boost DC /DC converter. Presence of overvoltage, even though they're reduced by the input voltage protection, can still damage semiconductor components, the transformer, the DC/DC link, or other circuitry or equipment connected to this converter, especially the boost converter used for PFC. For this reason, a sensor is introduced to detect such disturbances and shuts down part of the circuit if necessary.

IV. UPS WITH POWER FACTOR CORRECTION

A. Model of PFC

Power factor correction is achieved by introducing a DC/DC boost converter. The structure and arrangement of the boost converter in the overall system can be seen in Figure 11.

To control both current and voltage simultaneously, two control loops are used. The inner control loop is the current control loop and the outer one is the voltage control loop, as shown in Figure 10.

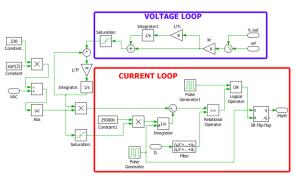


Figure 10: The boost DC/DC converter control schematic

The usual approach to control in PFC is cascade control with two PI controllers and PWM generator. However, in this case the occurrence of bifurcations is possible. To avoid this problem and achieve average current control (ACMC), peak current control (PCMC) with a low-pass filter in the feedback and an adaptive compensation ramp [10] is used, where the average current value is obtained by processing the feedback current signal with a low-pass filter. The time constant of the filter corresponds to switching frequency.

The requirement for obtaining the PFC is that the reference for the current through the inductor in the boost converter has the same waveform as the input voltage, i.e., a fully rectified sine wave. At the same time, the amplitude of this sine wave is determined by the output voltage of the boost converter. Thus, the reference for the inductor current is determined by multiplying the output of the voltage controller, a standard PI controller, by a rectified sine wave of amplitude 1 and the same frequency as the input voltage (100 Hz).

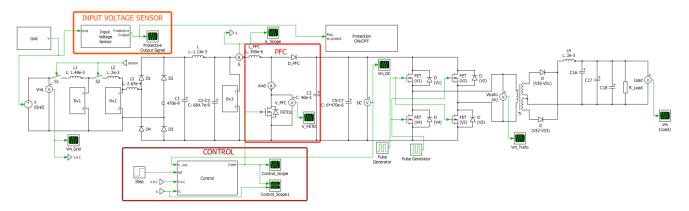


Figure 11: Complete model with PFC, PFC control and input voltage sensor

B. Input voltage disturbance sensor model

The PFC operate properly in the presence of nominal input voltage waveform. In the presence of distortions and overvoltages in the input voltage, the boost converter does not satisfactorily protect the circuits behind it. To achieve satisfactory protection, protection elements based on varistors and a detector of input voltage disturbance must be added. For this type of detection, a sensor has been developed whose only task is to detect the start of disturbances in the input voltage of the network and connect varistor-based protection elements before the boost converter. In this way, the rest of the system is protected from overvoltage and overcurrent. The block diagram of such a sensor is shown in Figure 12.

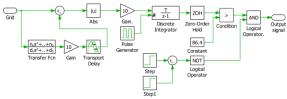


Figure 12: Input voltage disturbance sensor model

The output of the distortion sensor is based on the integral absolute error (IAE) between the actual input voltage and the first harmonic of the voltage. The first harmonic is obtained by a low-pass Butterworth filter with a cutoff frequency of 50 Hz (the frequency of the base harmonic), compensating gain and phase shift to maintain amplitude and phase equality with the original signal. The integrator is programmed to reset every 100 ms, which corresponds to 5 periods of input voltage. The 100 ms is the settling time of the IAE function and the Butterworth filter. This also means that the sensor operates with a sampling time of 100 ms. Comparing the IAE output signal to a threshold determines the presence of the distortion. If the output signal is greater than the threshold for the undisturbed signal, the input voltage is distorted for the last 5 periods and the sensor output signal changes from an initial 0, meaning no disturbance, to a 1. In the model, the sensor is disabled for the first 200 ms to prevent the sensor from responding to an initial transient response at power-up.

C. Voltage controller and simulation results

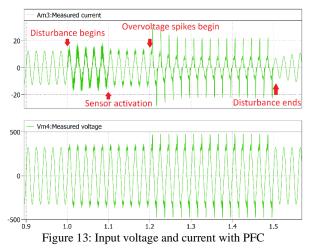
The controller in the outer loop of the boost converter cascade control is the voltage controller. The voltage controller of the PFC controls the output voltage of the PFC by influencing the sinusoidal current reference of the boost converter. It is designed as a PIT₁ controller with a time constant T_f equal to the period of the rectified input voltage of the boost converter to provide a smooth and undisturbed reference for the current controller during the input voltage period. The gain and integral time constant of the controller are determined by optimization using the Matlab/Simulink package and the optimization toolbox. The model for the optimization is based on the average boost converter model. Since the current model is much faster than the voltage part, the current part of the model is approximated by a current source controlled by a reference current signal. The gain K_r and the integral time constant T_i are determined by optimization using Newton based optimization function fmincon according to the ISE criterion, where the constraints are defined such that the rise time should be longer than 10 ms and the overshoot should be less than 1 %. These constraints and the filter of the controller guarantee the fastest disturbance compensation that does not affect the current shape required for the behavior of PFC.

TABLE 2: PARAMETERS OF THE EXISTING MODEL

Macromodel / Function	Element	Value
Control	K _r	2.2721
	T_i	0.2580 s
	T_f	0.01 s
	Current feedback filter	$13.33 \cdot 10^{-5} s$

Using the above parameters and the full model shown in Figure 11 the following results were obtained. Figure 13 shows the input voltage at PFC and the corresponding input current. In the beginning, the input voltage signal is sinusoidal and PFC controls the input current so that it is also sinusoidal and in phase. The total harmonic distortion (THD) in this case is 4.22 %, which is acceptable for a system with PFC. At the 1 second mark, higher harmonics as well as white noise are introduced

into the base sine wave signal. At 1.1 seconds, the voltage sensor detects the disturbance in the input signal and responds by activating inductors L1 and L2, which were previously deactivated.



From the 1.2 to 1.5-second mark, overvoltage spikes are added to the higher harmonics, so the peak current is larger (about 30 A). After the input disturbance disappears, the system returns to its previous state, where it functions as PFC.

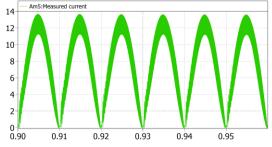


Figure 14: Current through inductor in the boost converter

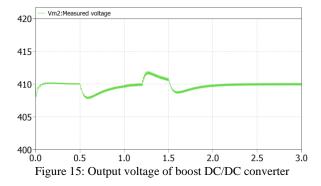


Figure 15 shows the output signal of the boost DC / DC converter. The set point for the output voltage is set to 410 V. At 0.5 s, a disturbance is applied in the form of a load change. The disturbance causes a current rise and an initial voltage drop. The controller compensates for the disturbance in about 0.5 seconds. At a time of 1.2 s the input voltage disturbance occurs (Figure 13) causing the output voltage to jump because the input voltage in the boost converter is greater than its output and the boost converter cannot operate under these conditions.

As soon as the disturbance ends and the input voltage drops, the output voltage returns to its set point.

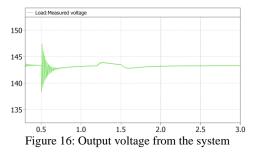


Figure 16 shows the output voltage of the system, and as can be seen, the system functions as UPS with minor disturbances when an additional load is introduced at 0.5 seconds. Figure 14 shows that the inductor current follows the given reference.

V. CONCLUSION

The protection against overvoltage and higher harmonics, which consists of varistors and inductors, successfully reduces the voltage stress on the components of the UPS. However, the introduction of the boost DC/DC converter into the system presents a new challenge, as a voltage sensor must be incorporated to detect the occurrence of higher harmonics and spikes in the input voltage so that the protection can be activated at the right time. As long as the overvoltage protection isn't in effect, the boost converter acts as PFC and does its job very efficiently, with the input current distortion factor being around 4.2 %.

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