Implementation of Voltage Regulation in a Spread-Spectrum-Clocked Buck Converter

Jurica Kundrata and Adrijan Barić
University of Zagreb, Faculty of Electrical Engineering and Computing, Unska 3, 10000 Zagreb, Croatia

***Abstract*—Buck converters use spread-spectrum technique to reduce the electromagnetic emissions by distributing the electromagnetic interference in a frequency band around the switching frequency which consequently reduces the amplitude of the interference. Changing the switching frequency also changes the output voltage and causes an unwanted output voltage ripple. The output voltage ripple is then reduced by properly controlling the time delay used in the duty cycle controller of the buck converter. This paper presents a digital implementation of the duty cycle controller used in the buck converter which uses a phase-locked loop to generate the switching frequency. Changing the divider value of the phase-locked loop changes its output frequency, but this frequency change is not instantaneous and it is modelled as a second-order system response. The implementation of the duty cycle controller presented and analysed in this paper aims to compensate for this transient change of the output frequency, i.e. the switching frequency and keep the duty cycle of the buck converter constant. The paper focuses on the compensation algorithm used to generate a constant duty cycle, as well as on the challenges of its digital implementation.**

***Index Terms*—DC-DC converter, spread-spectrum, duty cycle compensation, on-time compensation, physical implementation**

I. Introduction

Recent years have seen an increase in the switching frequency of switch-mode power DC-DC converters, which has led to the emergence of fully-integrated converters. These converters offer various advantages over discrete component designs, including simpler use, reduced cost, and improved reliability [1]. Efficiency is a crucial characteristic of power converters, and the utilization of resonant soft-switching techniques can reduce switching losses and maintain high efficiency even at switching frequencies of tens of MHz [2], [3], [4].

One of the significant challenges in designing high-frequency DC-DC converters is the increase in electromagnetic emissions resulting from the increased switching frequency. The generated electromagnetic emissions must not exceed the specified limits in regulations [5]. Regulatory tests for electromagnetic compatibility (EMC) have shown that even low-power devices with frequencies exceeding 160 MHz have failed such tests [6] [7].

Integrated converters offer another advantage in the form of advanced management techniques that can be used at a minimal cost, primarily related to silicon area. One such technique is the spread-spectrum modulator, which reduces electromagnetic emissions by distributing its energy to the frequency band around it. The magnitudes of the spread-spectrum frequency components are reduced compared to the magnitude of the original signal, although the total energy of the signal during modulation is not altered.

The spread-spectrum technique has become increasingly popular as an efficient means of reducing electromagnetic emissions [8]. Various switching devices already take advantage of this technique including SATA controllers [9], audio amplifiers [10], [11] and power converters [8], [12]. However, despite being widely used in commercial products, it has been demonstrated in [13] that the spread-spectrum technique's parameters are not always optimized for specific applications.

The use of spread-spectrum techniques is typically a trade-off, while it improves electromagnetic compatibility (EMC), it may worsen other device characteristics such as efficiency, output voltage ripple, etc. Moreover, a spread-spectrum technique effective in reducing conducted EM emissions may not be equally effective in reducing radiated EM emissions, and vice versa. However, a spread-spectrum modulation technique called Dual Random Spread Spectrum (DRSS) was recently introduced which is effective in reducing both conducted and radiated electromagnetic interference (EMI) [14]. Commercially available converters typically use fixed spread-spectrum modulation, with user-configurable parameters being unavailable. The introduction of a configurable spread-spectrum modulator would enable a better understanding of these trade-offs and enable optimization of EM emission reduction without compromising device performance. Although, there are commercially available devices in which the output ripple introduced by the spread spectrum is greatly reduced by using the feed-forward technique [15].

Application of the spread-spectrum technique in DC-DC converters leads to e.g. a substantial output voltage ripple as the duty cycle of the output voltage changes with the changing switching frequency. In [16] the output voltage ripple, as well as several compensation techniques are analysed.

This paper presents an integrated spread-spectrum controller design which uses a first-order approach to compensate the transient change of the output oscillator frequency used in a buck converter thus reducing its output voltage

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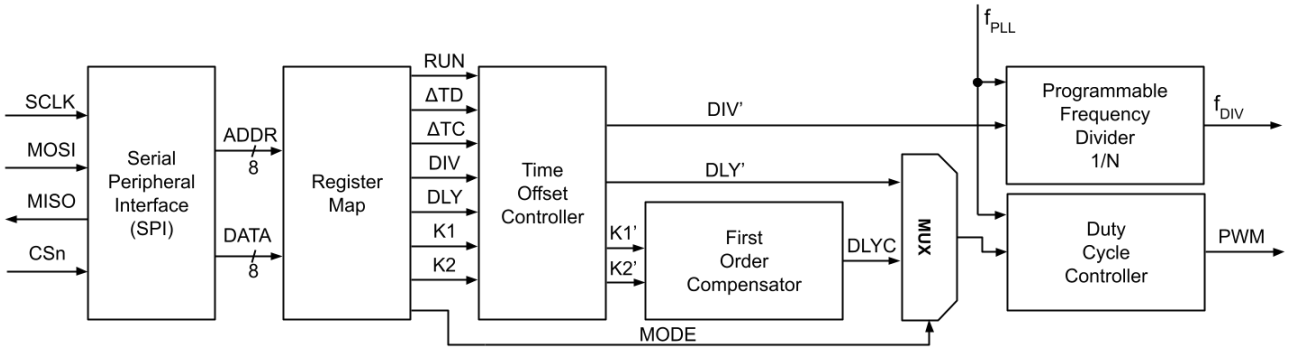

Fig. 1: The block diagram of the spread-spectrum controller including the first-order compensator.

ripple.

Section II presents the top level design of the spread-spectrum controller. Section III describes the design of the first-order compensator including its data flow. The spread spectrum controller is functionally verified by simulations in Section IV. Section V presents the physical implementation of the spread-spectrum controller followed by conclusions in Section VI.

II. Spread-spectrum controller

Fig. 1 shows the block diagram of the spread-spectrum controller including the first-order compensator. The spread-spectrum controller consists of the duty-cycle controller and the programmable frequency divider. The programmable frequency divider is connected in the feedback loop of an external Phase-Locked Loop (PLL) oscillator. The output frequency of the divider f_{DIV} represents the output frequency of the PLL oscillator f_{PLL} divided by a constant N and serves as the feedback signal in the PLL oscillator. The output frequency of the PLL oscillator is fed to the divider, but also to the duty-cycle controller which outputs a Pulse-Width Modulated (PWM) signal with a given value of the time-delay, i.e. the duty cycle. The output signal of the duty-cycle controller is used as the switching signal of the buck converter.

This spread-spectrum controller is designed to be used together with an external PLL oscillator and combining them with an output stage constitutes a complete buck converter controller.

The spread-spectrum controller is parametrized using the Serial Peripheral Interface (SPI). The communication interface itself consists of the clocking signal SCLK, chip select signal CSn and data-carrying signals MOSI and MISO. The spread-spectrum controller features an SPI slave which translates the SPI two-byte transfers to accesses to the register map. The individual SPI transfer consists of the address byte ADDR and the data byte DATA which are then used to configure the register map.

The parameters determined by the register map are fed to the time offset controller, first-order compensator, programmable frequency divider and duty cycle controller. The time offset controller uses timers which are loaded with the divider time offset ΔTD and compensator time offset ΔTC values. These values determine the time delays applied to the divider DIV, constant on-time delay DLY and compensator coefficients K1 and K2. The delayed parameters are respectively DIV', DLY', K1' and K2'. The time offset controller allows for fine tuning the start of the on-time compensation with respect to the PLL oscillators transient behaviour. The register map command RUN is used to start the time offset controller, while the command MODE is used to select the constant or compensator-generated DLYC on-time using the multiplexer shown in Fig. 1.

Table I shows the mapping of the register bank used in the spread-spectrum controller. The register map consists of 12 individual addresses where the first few addresses represent individual commands or values, while the rest of the addresses represent in pairs the high and low bytes of the parameters of the spread-spectrum controller. The address 0x00 represents the command RUN which enables/disables the operation of the spread-spectrum controller. The address 0x01 represents the mode selection command MODE which is used to select the operation mode of the spread-spectrum controller. There are two separate operation modes: the constant delay mode and the mode which uses the time delay values generated by the first-order compensator DLYC. The address 0x02 represents the divider value DIV used in the frequency divider of the PLL oscillator. The following addresses represent the lower and higher bytes of the constant time delay value DLY, first-order compensator constants K_1 and K_2 and accompanying time offset values for the divider ΔTD and first-order compensator ΔTC.

III. First-order compensator

This paper uses an exponential compensation technique of the on-time t_{ON} which uses a straightforward difference equation defined as

$$t_{ON}[n] = t_{ON}[n-1] + \frac{T_{CLK}}{\tau_C}(t_{ON,trgt} - t_{ON}[n-1]) \quad (1)$$

where $t_{ON}[n]$ and $t_{ON}[n-1]$ are the compensated on-time values at two consecutive calculation steps, T_{CLK} is the

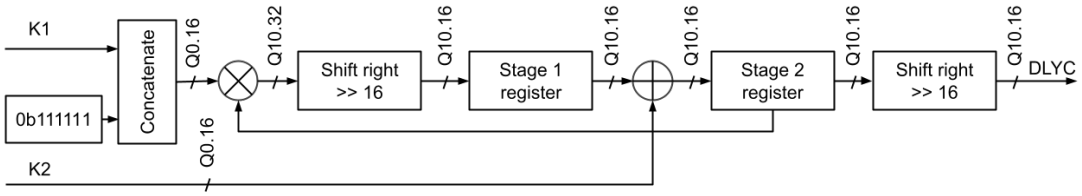

Fig. 2: The data flow of the first-order compensator.

time period of the controller clock, τ_C is the time constant of the exponential compensation technique and $t_{ON,trgt}$ is the targeted, final value of the compensated on-time value. The difference equation includes three arithmetic operation, i.e. subtraction, multiplication and addition. The difference equation can be reorganized in order to reduce the number of necessary operations and consequently simplify the digital implementation of the first-compensator. The simplification of the difference equation begins by expanding it as follows

$$t_{ON}[n] = t_{ON}[n-1] + \frac{T_{CLK}}{\tau_C} t_{ON,trgt} - \frac{T_{CLK}}{\tau_C} t_{ON}[n-1] \tag{2}$$

which leads to

$$t_{ON}[n] = t_{ON}[n-1]\left(1 - \frac{T_{CLK}}{\tau_C}\right) + \frac{T_{CLK}}{\tau_C} t_{ON,trgt} \tag{3}$$

and finally

$$t_{ON}[n] = K_1 \cdot t_{ON}[n-1] + K_2 \tag{4}$$

where

$$K_1 = 1 - \frac{T_{CLK}}{\tau_C} \text{ and } K_2 = \frac{T_{CLK}}{\tau_C} t_{ON,trgt} \tag{5}$$

where $t_{ON,trgt}$ is defined as

$$t_{ON,trgt} = \frac{D}{f_{SW}} \tag{6}$$

TABLE I: THE REGISTER MAPPING.

Address	Register Name	Register Description
0x00	RUN	Run command
0x01	MODE	Operation mode
0x02	DIV	Divider value
0x03	DLY_L	Constant delay, L byte
0x04	DLY_H	Constant delay, H byte
0x05	K1_L	Compensator constant K_1, L byte
0x06	K1_H	Compensator constant K_1, H byte
0x07	K2_L	Compensator constant K_2, L byte
0x08	K2_H	Compensator constant K_2, H byte
0x09	ΔTD_L	Divider time offset, L byte
0x0A	ΔTD_H	Divider time offset, H byte
0x0B	ΔTC_L	Compensator time offset, L byte
0x0C	ΔTC_H	Compensator time offset, H byte

where D is the targeted duty cycle of the buck converter output and f_{SW} is the switching frequency of the buck converter, i.e. the output frequency of the PLL oscillator f_{PLL}.

Fig. 2 shows the data flow of the first-order compensator. The data flow implements the sequence of the operations required to calculate the next time delay value as defined in relation (4). Furthermore, the two operations, i.e. the multiplication and addition are separated each in its own stage which constitutes a pipeline and facilitates the time closure of the digital design during synthesis.

The first-order compensator is designed to use a fixed-point fractional number format. The width of the output time delay value is determined by the size of the control word of the duty cycle controller, while the widths of the input constants K1 and K2 are chosen with respect to the value changes with the used time steps. Both constants K1 and K2 are less than 1 and consequently the Q0.16 number format is used. Additionally, constant K1 is very close to 1 as it will be shown in Section IV and the upper 6 bits of constant K1 are fixed. This is represented by the concatenation block in Fig. 2. Fixing the upper bits of the constant K1 also simplifies the synthesis of the following multiplication block.

The generated time delay value is internally kept in the Q10.16 format in order to preserve the accuracy of the calculation and to accommodate the small value changes due to very small ratio of the clock period and time constant, also discussed in Section IV. Consequently the output of the multiplication block is Q10.32 which is rounded to the Q10.16 format using the following shift right block. The value of the multiplication is kept in the Stage 1 register. The value of the Stage 1 register is then used in the addition with constant K2 which results in the internal value of the time delay and it is kept in the Stage 2 register. The output time delay value DLYC is finally generated by rounding the Stage 2 register value using the following shift right block.

IV. Digital simulation

The digital core which implements the spread-spectrum controller is functionally verified by digital simulation. The digital simulation is based on a testbench which communicates with the spread-spectrum controller via the SPI communication interface and sets the parameters of the first-order compensator for the testcase where the output PLL frequency starts at the mean value, then reduces to

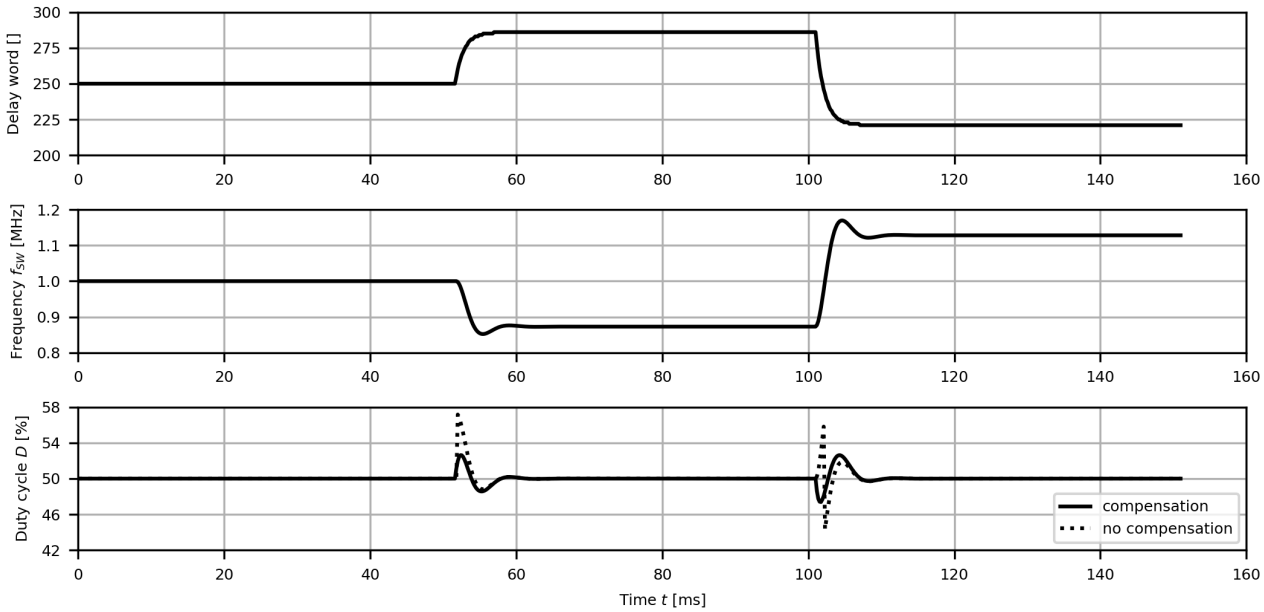

Fig. 3: The waveforms of the simulated compensator-generated delay word, switching frequency and resulting duty cycle.

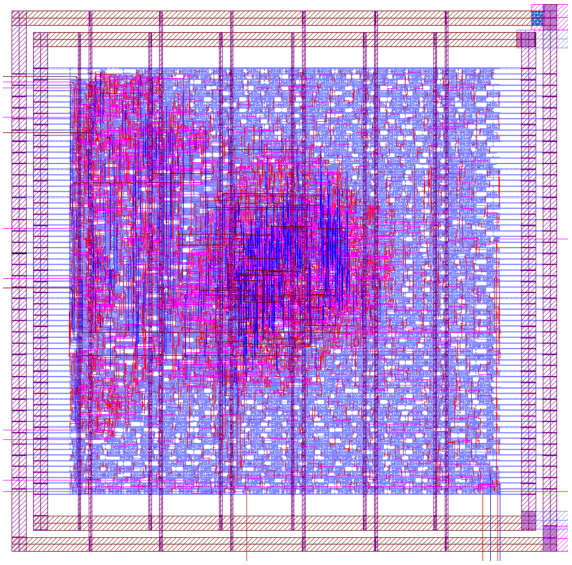

Fig. 4: The layout of the spread-spectrum controller.

the minimum value and finally increases to the maximum value.

Table II shows the parameters of the first-order compensator used in the testbench simulations. The testbench simulation uses three distinct PLL frequencies to illustrate the functioning of the first-order compensator. The simulation starts at the nominal frequency f_{PLL} = 1 MHz, in the next part of the simulation it drops to the minimum value f_{PLL} = 0.873 MHz and finally it steps up to the maximum value f_{PLL} = 1.128 MHz. The target delay times $t_{ON,trgt}$ shown in Table II are calculated using (6). The delay words DLY are the control words used in the digital spread spectrum controller to represent the given delay time $t_{ON,trgt}$ and they are calculated using

$$DLY = \lfloor \frac{t_{ON,trgt}}{\Delta t} \rfloor \tag{7}$$

where the resolution of the duty cycle controller is Δt = 2 ns which is defined by the used delay standard cell.

The parameters of the first-order compensator in Table II are calculated using (5) where the clock frequency, i.e. its period is T_{CLK} = 1 ns and the time constant τ_C = 1.25 ms. Furthermore, these parameters are presented in their fixed-point fractional number formats as used in the first-order compensator.

Fig. 3 shows the waveforms of the simulated compensator-generated delay word, switching frequency and resulting duty cycle. The upper waveform represents the delay words generated by the first-order compensator. The middle waveform shows the switching frequency generated by an example PLL oscillator which features the characteristic second-order transient change. The lower waveform shows the resulting duty cycle of the output PWM signal for the cases without (command MODE = 0) and with (command MODE = 1) first-order compensation. The resulting duty cycle is calculated using

TABLE II: THE COMPENSATOR PARAMETERS.

Frequency f_{SW} [MHz]	**0.873**	**1.0**	**1.128**
Delay time $t_{ON,trgt}$ [ns]	572	500	444
Delay word DLY []	286	250	222
Parameter $K1$ []	0.9992	0.9992	0.9992
Parameter $K2$ []	0.2288	0.2000	0.1776
Parameter $K1$ [Q0.16]	0xFFCB	0xFFCB	0xFFCB
Parameter $K2$ [Q0.16]	0x3A92	0x3333	0x2D77

TABLE III: THE AREA UTILIZATION OF THE SPREAD-SPECTRUM CONTROLLER.

Type	Instances	Area [μm^2]	Area [%]
Sequential	290	15950.323	22.4
Inverter	94	623.437	0.9
Buffer	1025	38222.823	53.8
Logic	1036	16290.579	22.9
Total	2445	71087.162	100.0

TABLE IV: THE AREA UTILIZATION OF THE FIRST-ORDER COMPENSATOR.

Type	Instances	Area [μm^2]	Area [%]
Sequential	52	2638.630	17.2
Inverter	81	533.434	3.5
Buffer	3	26.342	0.2
Logic	734	12102.138	79.1
Total	870	15300.544	100.0

$$D = DLY \cdot \Delta t \cdot f_{SW}. \tag{8}$$

The comparison of the output duty cycle in the cases with and without the first-order compensation in Fig. 3 shows that the duty cycle error is approx. $\pm 6\%$ when no compensation is used and it is approx. $\pm 2.5\%$ when the first-order compensation is used.

V. Physical Implementation

The spread-spectrum controller with the SPI communication interface and first-order compensator as shown in Fig. 1 is physically implemented in the 180-nm TSMC technology. Fig. 4 shows the layout of the physical implementation of the spread-spectrum controller. The size of the digital core including the power ring is approx. 400 by 400 μm^2. Most of the area in the digital core is taken up by the duty cycle controller and the delay cells it uses. The purple-coloured area in the layout corresponds to the area taken by the delay cells, while the red-coloured area corresponds to the rest of the logic of the digital core.

Table III shows the area utilization of the physical implementation of the spread-spectrum controller. Table shows that the digital core has a large number of buffer cells which take up more than half of the total cell instances and area. These buffer cells are mostly delay cells used by the duty cycle controller as observed earlier in Fig. 4. Rest of the cells used by the digital core are approximately evenly distributed between the sequential and logic standard cells and they implement the rest of the digital blocks shown in Fig. 1.

Table IV shows the area utilization of the physical implementation of the first-order compensator alone. Table shows that the first-order compensator constitutes approx. a third of the standard cell instances and approx. a fifth of the utilized area of the whole spread-spectrum controller. The difference in these ratios is due to the fact that the delay cell used in the duty cycle controller has a significantly larger area than the rest of the standard cells. The number of the sequential standard cells correspond to the Stage 1 and Stage 2 registers which hold the intermediary values in Q10.16 format. The logic standard cells implement the arithmetic operations of multiplication and addition in each stage. The physical implementation of this digital core estimates a power consumption of 42 μW.

VI. Conclusions

Spread-spectrum technique is used in buck converters to reduce electromagnetic emissions. However, changing the switching frequency to implement this technique causes unwanted output voltage ripple, which can be reduced by controlling the time delay used in the duty cycle controller. The paper presents a digital implementation of the spread-spectrum controller, which includes a first-order compensator of the on-time used in the duty cycle controller. The implementation aims to compensate for the transient change of the output frequency and keep the duty cycle of the buck converter constant. The first-order compensator uses a difference equation to generate new on-time values which is implemented in a pipeline with reduced number of arithmetic operations with a fixed-point fractional number representation. The spread-spectrum controller design is functionally verified by simulations which show that the compensator can reduce the duty cycle error by more than half. The physical implementation results show that the addition of the first-order compensator to the spread-spectrum controller increases the area of the implemented core by a quarter, while providing the reduction of the output voltage ripple of the buck converter.

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