Developing a Model of Buck Converter for EMI Filter Optimization by Circuit Simulations

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***Abstract*—Switching DC-DC converters for automotive applications typically require an input EMI filter to comply with the regulations. An automotive buck converter with the 5-A maximum output current is designed. To validate the performance, the buck converter is modelled in the circuit simulator. The model consists of the power stage and the voltage-mode control loop. Discrete components are modelled by real models with parasitic elements. The performance of the converter without the EMI filter is provided.**

Keywords—voltage-mode control loop, parasitic elements, conducted emissions

I. INTRODUCTION

Most of electronic devices are affected by electromagnetic interference (EMI) in the presence of electromagnetic waves caused by a source device or proximity device which is an operational disturbance. This can cause malfunction or unwanted operation of electronic circuits and components. EMI control is one of the more difficult challenges in switching DC-DC converter design, beyond functional issues, robustness, cost, thermal and space constraints. The most commonly used switching DC-DC converter is a buck converter, which down-converts a DC voltage to a lower DC voltage of the same polarity [1]. The main components of the power stage of synchronous buck converter are the high-side and low-side power MOSFET, with the output low pass filter which consists of the power inductor and output capacitor [2]. The synchronous buck converter uses high-side and low-side MOSFET as a switch that alternately connects and disconnects the input voltage to an inductor.

This paper is organized as follows. Section II describes the buck converter circuit. Selection of the main components and voltage-mode control loop design are presented in Section III. Simulations of the designed buck converter are shown and discussed in Section IV. Finally, a conclusion is given in Section V.

II. BUCK CONVERTER CIRCUIT

By using design requirements, such as the input and output voltage, operating frequency, the values of components in the output filter are determined, and power MOSFETs are selected. The selection of inductor above the critical value makes the buck converter operate in continuous-conduction mode and determines the output ripple current while the output capacitance directly affects the output voltage ripple and loop stability with the overshoot and undershoot during load transients [3]. After selection of the main components in the power stage, a voltage reference, an error amplifier and delay circuit must be added to the the power stage in order to regulate the output voltage. The complete buck converter circuit combined of these basic blocks is shown in Fig. 1.

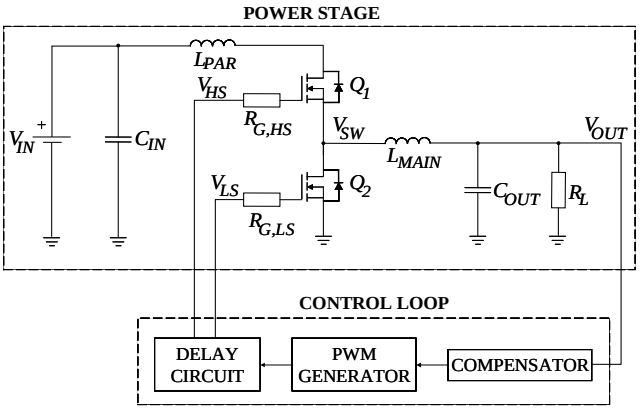


Fig. 1: Synchronous buck converter with voltage-mode control loop.

Conducted emissions are divided into differential-mode and common-mode interference [4]. Differential-mode interference is a noise signal which exists between line and return conductors. In contrast, common-mode noise is a signal which is in-phase on both the line and return conductors reffered to the safety ground. The focus is on conducted EMI in switching DC-DC converters generated by high current transients at the input and switching actions of the power MOSFETs.

III. BUCK CONVERTER DESIGN

A. Power MOSFET's model

When a MOSFET is used as a switch, its basic function is to control the drain current by the gate voltage. Fig. 2 shows the model of a power MOSFET. In order to model the power MOSFET, the voltage-contolled switch SW_1 with the on-state resistance R_{ds} is connected in series. Due to their structure, MOSFETs have parasitic capacitances and the switching performance of the device is determined by the time required to establish voltage across the parasitic capacitances [5]. In additon to the on-

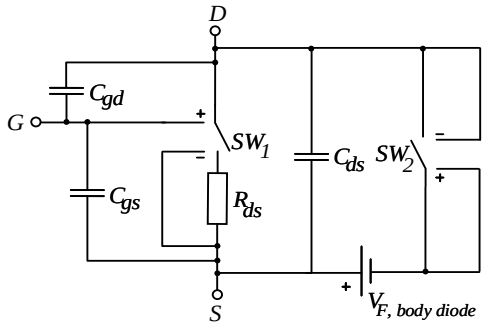


Fig. 2: Power MOSFET model.

state resistance, the gate-to-source capacitance C_{gs}, the gate-to-drain capacitance C_{gd} and the drain-to-source capacitance C_{ds} have been added to the model. Furthermore, due to p-n junction between the source/drain and the bulk, MOSFETs have an intrinsic body diode providing a path for inductive load current to bypass the MOSFET during the off-state. The body diode is modelled by using the voltage-controlled switch SW_2 and the 0.7-V reference voltage $V_{F,bodydiode}$. The MOSFET parameters selected from the automotive-compliant, 5 A, synchronous buck converter AP64502Q [6] are shown in Table I.

TABLE I: MOSFET parameters

Parameter	high-side MOSFET	low-side MOSFET
R_{ds}	45 mΩ	20 mΩ
C_{gs}	90 pF	200 pF
C_{ds}	350 pF	200 pF
C_{gd}	25 pF	20 pF

B. Inductor, input and output capacitor selection

Design parameters:

- Output voltage, V_{OUT} = 5 V
- Maximum load current, $I_{OUT_{max}}$ = 5 A
- Switching frequency, f_{sw} = 2.2 MHz
- Nominal input voltage, $V_{IN_{nom}}$ = 14 V
- Input voltage range, V_{IN} = 6 V to 28 V
- Duty cycle, D = 0.36
- Transient load step, I_{step} = 2.5 A
- Voltage overshoot V_{OS} = 1.03 · V_{OUT} = 5.15 V

Design requirements:

- Inductor peak-to-peak ripple current, $\Delta I_{L_{pp}}$ = 1 A
- Output peak-to-peak ripple voltage, $\Delta V_{OUT_{pp}}$ = 20 mV
- Allowed input peak-to-peak ripple voltage, $\Delta V_{IN_{pp}}$ = 100 mV

The required inductance is calculated from the desired peak-to-peak ripple current. The higher the inductor value, the higher is the output current because of the reduced ripple current. Commonly, the lower the inductor value, the smaller is the solution size. The following equation shows the needed inductance for the ripple current [3]:

$$L_{MAIN} > \frac{V_{OUT} \cdot (V_{IN_{nom}} - V_{OUT})}{\Delta I_{L_{pp}} \cdot f_{sw} \cdot V_{IN_{nom}}} \quad (1)$$

The inductance should be greater than 1.46 µH as calculated by (1). The inductor must always have a higher current rating than the maximum load current of 5 A due to current increase with decreasing inductance. A 1.5 µH Coilcraft power inductor from the XEL series is selected [7]. Parasitic elements of the inductor include the resistive element R_{DC} in series and the parallel capacitance $C_{P,MAIN}$ with the series resistance $R_{S,MAIN}$. To complete the model of the inductor, the parallel resistance $R_{P,MAIN}$ is added. Fig. 3 (a) shows the inductor model. The values of the parasitic frequency-dependent elements are calculated from [7], as shown in Table II.

TABLE II: Inductor parasitic elements (Coilcraft inductor)

Inductor	R_{DC}	$C_{P,MAIN}$	$R_{S,MAIN}$	$R_{P,MAIN}$
L_{MAIN}	4.5 mΩ	12 pF	30 Ω	1400 Ω

Due to the maximum output current $I_{OUT_{max}}$ of the DC-DC switching converter for a given application, the minimum value of the input capacitor is critical for stabilizing the input ripple voltage. Equation (2) estimates capacitance C_{IN} that will meet the ripple requirement [2]:

$$C_{IN} > \frac{D \cdot (1 - D) \cdot I_{OUT_{max}}}{f_{sw} \cdot \Delta V_{IN_{pp}}} \quad (2)$$

The input capacitance should be greater than 5.4 µF. With two 4.7 µF capacitors in parallel, the total effective capacitance is sufficient for stabilizing the ripple voltage.

Commonly the selection of the output capacitor is not driven by the desired ripple voltage, but by the load transient response. The output voltage fluctuates due to the time it takes the inductor to catch up with the increased or decreased output current. An empirical formula (3) is used to calculate the necessary output capacitance for the specified output overshoot or undershoot [8]:

$$C_{OUT} > \frac{I_{step} \cdot (\frac{1}{4 \cdot f_c} + \frac{1}{f_{sw}})}{2 \cdot V_{OS}} \quad (3)$$

A good starting value for the crossover frequency f_c is 1/20 to 1/10 of the switching frequency f_{sw}. For this application, f_c = 1/20 · f_{sw} = 110 kHz is selected. The minimum output capacitance C_{OUT} for the 3 % output voltage change with the crossover frequency f_c of 110 kHz is 22.7 µF. Connecting three 10 µF capacitors in parallel is enough to supply the current difference to maintain the output voltage within the specified range. Table III shows the chosen Murata MLCC capacitors parasitic elements from the GCM series.

The input and output capacitors are modelled with parasitic elements. The impedance-frequency characteristic is used for extracting equivalent series resistance (ESR) and the equivalent series inductance (ESL) of the output capacitors [9]. Real model of the capacitor with parasitic elements is shown in Fig. 3 (b).

TABLE III: Input and output capacitor parasitic elements (Murata MLCC capacitors)

Capacitor	ESL	ESR
4.7 µF (C_{IN} = 2×4.7 µF)	0.6 nH	4 mΩ
10 µF (C_{OUT} = 3×10 µF)	0.7 nH	3 mΩ

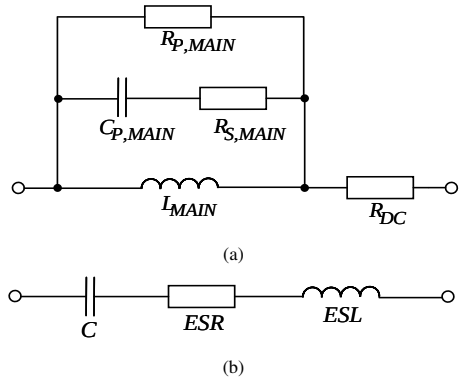


Fig. 3: Parasitic elements of the components. (a) Model of the inductor. (b) Model of the capacitor.

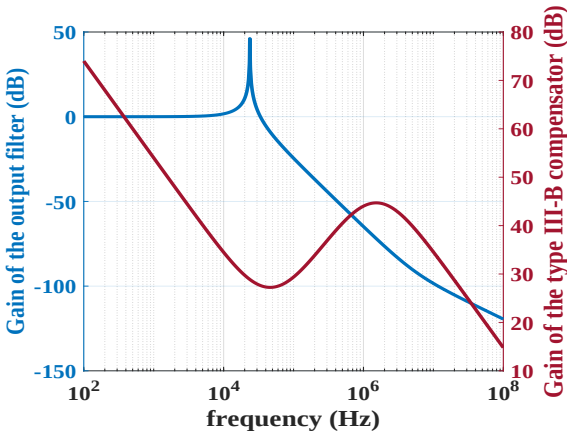


Fig. 4: Simulation of the amplitude-frequency chacteristic of the output filter and amplitude-frequency chacteristic of type III-B compensator for determined zeros and poles. The first zero of the compensator (f_{z1}) compensates the phase lag of the pole which is at the origin. The second zero (f_{z2}) is to compensate for one of the poles of the LC filter so that at f_c the slope of the bode plot of the loop is about -20 dB/dec. The second pole of the compensator (f_{p2}) and the zero of the ESR of the capacitor (f_{ESR}) cancel each other and the third pole (f_{p3}) is to provide more attenuation for frequencies above f_s/2.

C. Voltage-mode control loop design

In voltage-mode control the output voltage is returned through a feedback loop. The differential voltage, which is obtained to compare the output voltage with the reference voltage by an error amplifier, is compared with the triangular waves by a PWM generator [10]. As a result, the pulse width of the PWM signal is determined to control the output voltage.

In order to ensure a stable system, a slope of the loop gain should be about -20 dB with a phase margin greater than 45 ° for the overall stability. To make the analysis of the compensation network simpler, the ESL of the output capacitor and the series resistance R_{DC} with other parasitic elements of the output inductor are neglected. The transfer function of the output filter is a second order system with a double pole at a resonance frequency of the LC filter and a zero produced by the ESR of the output capacitor, as shown in Fig. 4. The double pole at 23.7 kHz causes the gain to fall with a slope of -40 dB/dec up to zero frequency of 5.3 MHz which compensates one of the poles.

As mentioned, having a stable closed loop buck converter with an appropriate performance, a properly designed compensator is required. The feedback is implemented with a type III-B compensation network [10] due to location of the desired zero crossover frequency f_c = 110 kHz, switching frequency f_{sw} = 2.2 MHz and charasteristics of the output filter. Using equations described in [10], the desired locations of the poles and zeros of the compensator are calculated. Fig. 4 shows the amplitude-frequency charasteristic of the type III-B compensator. Furthermore, the resistors and capacitors of the compensator (see Fig. 5) with the closest standard components values to the calculated results for achieving detemined poles and zeros are shown in Table IV.

TABLE IV: Values of parameters in compensation network

Parameter	Value
R_{F1}	23.7 kΩ
R_{F2}	3.83 kΩ
R_{F3}	768 Ω
C_{F3}	0.1 nF
R_{C1}	374 kΩ
C_{C1}	13 pF
C_{C2}	0.39 pF

An error amplifier added between the regulator output and the PWM generator holds the output voltage constant and controls the duty cycle of the PWM signal providing required gain and phase of the loop so desired phase margin and zero crossover frequency are attained. The error amplifier is implemented using an operational amplifier modelled by the input and output resistance with a voltage-controlled voltage source. In order to close the loop of the buck converter, the PWM generator is inserted so that a repeating rectangular output waveform in response to a control voltage is produced. As the control voltage increases, the duty cycle of the output increases as well. When the control voltage is greater than the voltage of the ramp signal, the output is continuously high. In contrast, the output of the comparator is continuously low if the control voltage is below the ramp voltage. The PWM generator is achieved by a sawtooth waveform with the peak voltage V_{OSC} = 5 V and the comparator modelled by the operational amplifier, as shown in Fig. 6.

When both the high-side MOSFET Q_1 and low-side MOSFET Q_2 turn on simultaneously, shoot-through happens which means the input voltage will be shorted to the ground. To prevent shoot-through, a delay circuit is required. After one MOSFET turns off, delay circuit will generate a short dead time t_d before another MOSFET

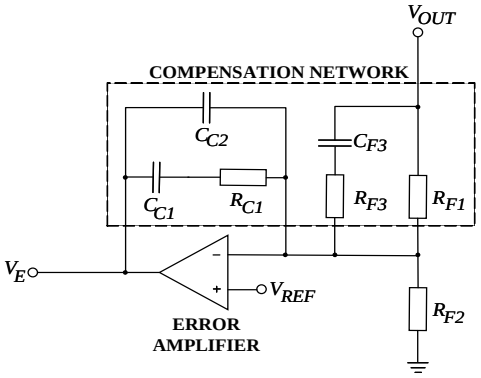


Fig. 5: Type III-B compensator.

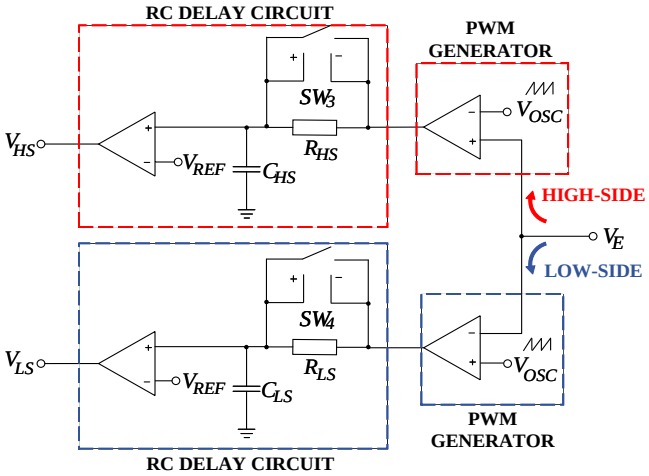


Fig. 6: RC delay circuit with PWM generator.

switches on. The inductor current will be conducted by the body diode of the low-side MOSFET to keep the current continuos during the dead time when both the high-side and low-side are off. Fig. 6 shows the delay circuit. The main component of the delay generator is an RC circuit in parallel with the Schottky diode modelled by the voltage controlled switches SW_3 and SW_4. At the output of the comparator, due to PWM signal's falling edge, the diode conducts and the circuit adds no delay due to very small RC constant. In contrast, during the falling edge of the PWM signal, the Schottky diode is bypassed and the RC circuit converts the PWM signal edge into the ramp signal. Inserting the voltage comparator between the delay circuit and the MOSFET gate resistance, the output ramp is flipped at V_{REF} = 3 V to ensure lagging of the delay circuit output rising edge compare to the PWM signal rising edge. The values of parameters in the RC circuit are shown in Table V.

TABLE V: RC contants for the high-side and low-side MOSFET

Parameter	HS MOSFET	LS MOSFET
R	47 Ω	47 Ω
C	127 pF	150 pF
t_d	5.2 ns	10.1 ns

Different RC constants for the high-side and low-side MOSFET are selected, essentially different dead times t_d (see Fig. 8), to have body diodes conducting about 5 ns.

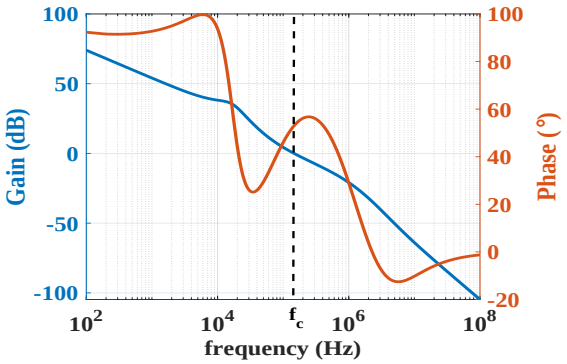


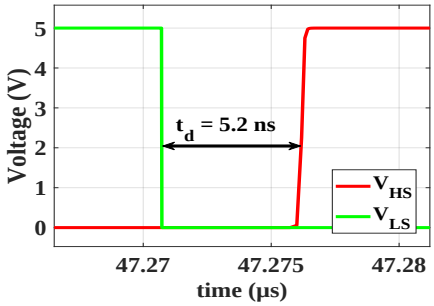
Fig. 7: Simulation of the Bode plot of the loop gain with the slope at crossover frequeny of -20 dB/dec and the phase margin of about 51 °.

Fig. 7 shows the Bode plot of the developed buck converter loop gain.

IV. SIMULATION ENVIRONMENT AND RESULTS

In order to verify the efficieny of the designed buck converter, the *Advanced Design System* (ADS) model is created. The simulation model, as shown on Fig. 1, has been operated under full load conditions, continuous current mode and closed loop control. The external 2-Ω gate resistors $R_{G,HS}$ and $R_{G,LS}$ are very important in limiting noise and ringing due to the parasitic capacitances and inductances, high voltage and current change that can cause unwanted performance. Small resistor values result in faster turn-on speed, but can cause the overshoot in the gate voltage. However, higher resistor values overdamp the oscillation and extend the switching time. Also, due to the parasitic elements on the printed circuit boards, the inductor L_{PAR} = 1 nH placed between the power supply and high-side MOSFET Q_1 generates high frequency ringing. For the proper performance of the buck converter, the PWM generator must apply the square wave voltage with the 5-V peak across the gate of MOSFETs with the delay time inserted between the high-side MOSFET Q_1 and low-side MOSFET Q_2 switch over, defined as dead time (see Fig. 8). The results of the model simulations are shown in Fig. 9.

Fig. 9 (a) shows that the output voltage V_{OUT} equals 5.03 V. The voltage spikes with 50 mV peak are caused by equivalent series resistance (ESR) of the output capacitors. As seen in Fig. 9 (b) while the high-side MOSFET is in on-state, the inductance current increases due to constant positive voltage across inductor. In contrast, negative voltage causes current decrease during the on-state of the low-side MOSFET. In addition, inductor current ripple of 1 A is as required. The switch node alternatly connects to the input voltage $V_{IN_{nom}}$ = 14 V or ground, and rings to about 9 V larger voltage than the input voltage, as shown in Fig. 9 (c).



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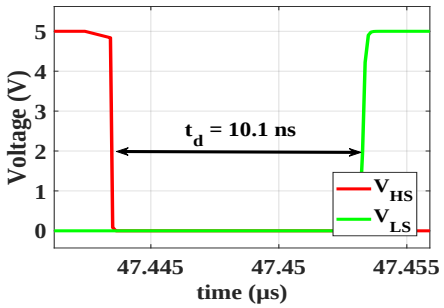


(b)

Fig. 8: (a) Simulation of the dead time from low-side MOSFET off to high-side MOSFFET on. (b) Simulation of the dead time from high-side MOSFET off to low-side MOSFET on.

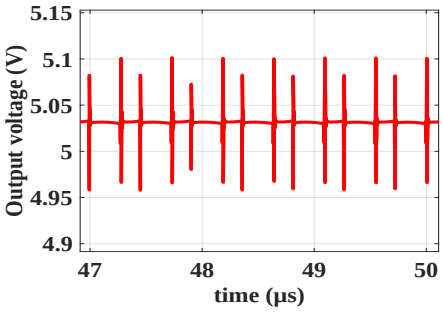
A. Load transient response

The performance of the feedback loop compensation and its stability can be tested by the transient response. The output of the under-compensated converter tends to oscillate, while the output of an over-compensated converter takes a long time to return to a steady state. The load transient response to a 2.5 A load step is shown in Fig. 10. The simulated voltage overshoot is about V_{OS} = 5.063 V.

B. Conducted emission

The input port EMI noise comes from voltage ripple generated by the discontinuous current on the input capacitors. The fundamental frequency of the voltage ripple is the switching frequency f_{sw} = 2.2 MHz of the designed buck converter. Higher order harmonics of the fundamental frequency also exist in the noise spectrum. For consistent results, conducted EMI measurments are performed using a passive device called a LISN (Line Impedance Stabilization Network) which establishes a consistent source and measurement impedance allowing for repeatability of test results. The LISN is connected in series with the power supply to the DC-DC switching converter. The topology of 5-µH LISN is shown in Fig. 11.

To measure or simulate conducted emissions, two seperate CISPR 25 LISN circuits are connected to the positive and negative power supply lines referenced to the ground plane. In additon, as seen in Fig. 12, the parasitic capacitance C_{PAR} = 100 pF is connected between the negative power supply line and reference ground plane.



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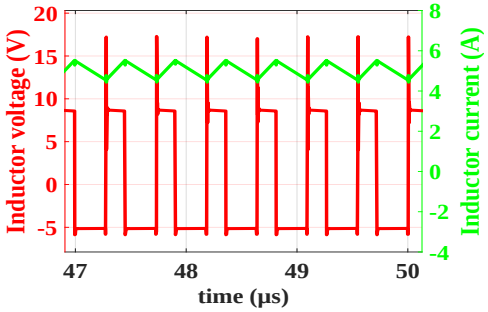

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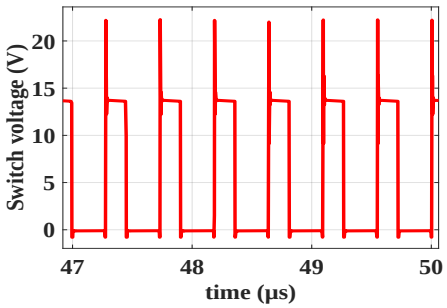


(c)

Fig. 9: Simulated results. (a) Output voltage V_{OUT}. (b) Inductor current I_L and voltage V_L. (c) Switch voltage V_{SW}.

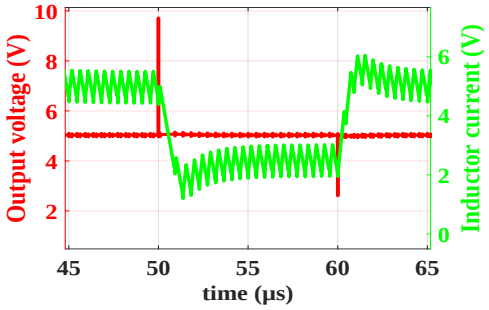
The most commonly used EMI measurement and conformance for automotive application standard is CISPR 25 which specifies limits of conducted EMI noise over a frequency range from 150 kHz to 108 MHz for peak (PK) and average (AVG) signal detectors. Fig. 13 shows the simulated differential-mode and common-mode conducted emissions described as

$$V_{DIFF} = V_{LINE,1} - V_{LINE,2}, \tag{4}$$

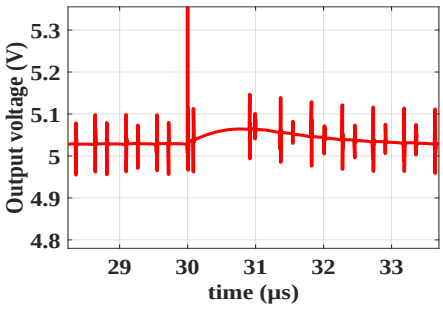
$$V_{COMM} = \frac{V_{LINE,1} + V_{LINE,2}}{2}, \tag{5}$$

where $V_{LINE,1}$ and $V_{LINE,2}$ are the noise voltages on the positive and negative power supply lines.

The most significant noise magnitude of 83.6 dBµV appers at the switching frequency f_{sw} = 2.2 MHz as expected. It is evident that the designed buck converter does not conform to CISPR 25 Class 5 standards. Therefore, in



(a)



(b)

Fig. 10: Simulated results. (a) Load transient response, I_L = 5 A to 2.5 A to 5 A. (b) Output voltage overshoot fits the calculated value.

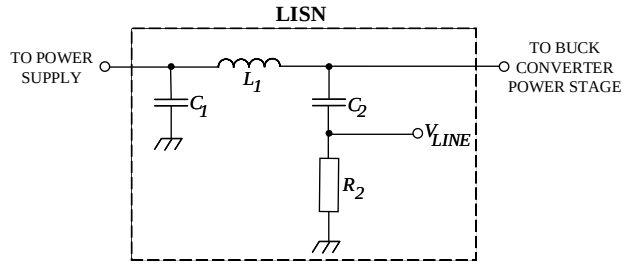


Fig. 11: LISN (Line Impedance Stabilization Network).

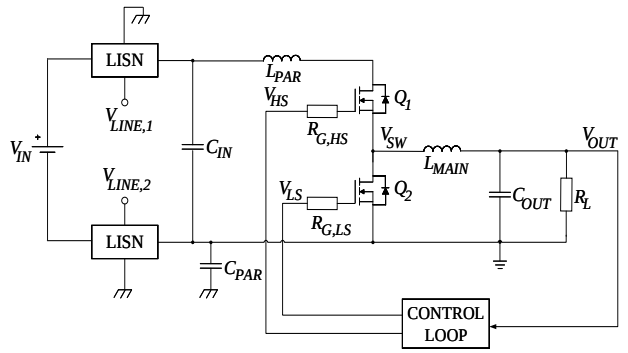


Fig. 12: Synchronous buck converter with voltage-mode control loop and LISN.

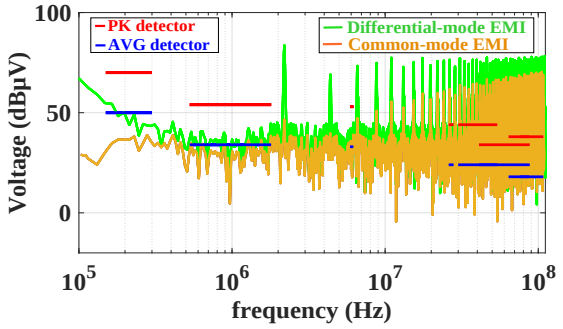


Fig. 13: Simulation of the differential-mode and common-mode conducted emissions.

order to satisfy the standard, the input EMI filter must be included in the design to reduce conducted emissions.

V. Conclusion

The model of a 5-A buck converter used for automotive applications is designed using Advanced Design System (ADS). The developed model consists of the power stage and voltage-mode control loop. The passive components are modelled by the model with parasitic elements using impedance-frequency characteristic. The buck converter performs as expected. Adding differential-mode EMI filter is required in order to reduce conducted emissions.

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