Design and Characterization of the Output Network of a High-Current Buck Converter

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***Abstract*—A 10-A automotive buck converter is designed and realized on a four layer printed circuit board. The output network is designed in the electromagnetic solver to account for the trace and package parasitic elements. The output network of the converter is simulated in the SPICE solver. The converter is characterized in the time domain by the load transient measurements and in the frequency domain by the shunt measurement method. Three configurations of the output network are compared. The results in the frequency domain and the results of the SPICE simulations are correlated.**

Keywords—automotive, PDN, target impedance, VRM, voltage overshoot

I. INTRODUCTION

Nowadays there is an increasing need for high current power supply that can power up different types of microcontrolers, processors and other electronics [1]. Efficiency of about 90% and higher is the main reason why DC-DC converters are commonly used for this purpose [2]. Buck converter is a form of DC-DC converter used for reducing the applied DC input voltage level to desired output voltage level. Buck converter is a part of a power distribution network (PDN).

The objective of the PDN is primarily to provide clean and reliable power to the active devices on the system. The PDN consists of the chip-level power distribution with thin-oxide decoupling capacitors, the package-level planes and mid-frequency decoupling capacitors and board-level power distribution with planes, low-frequency ceramic and bulk decoupling capacitors, and the voltage regulator module (VRM) [3]. Design of the PDN is typically done in the frequency domain by analyzing the impedance profile. Accurate method for characterization of low-impedance PDN is two-port shunt method. Main advantage of this method is reduced effect of series connection [4].

The second chapter describes the target impedance and the output network of the buck converter. Designed printed circuit board (PCB) of the buck converter with three versions of output network are presented. In chapter III, the results of simulation and measurements of the PDN impedance profiles are correlated. The load transient measurements and efficiency of buck converter for three versions of the output network are shown. Chapter IV concludes the paper.

II. POWER DISTRIBUTION NETWORK

A. Target impedance, output capacitance and inductor

The target impedance sets the limit on the highest impedance of the power rail for desired voltage change due to the amount of current drawn trough the rail. The objective is to have the output impedance below the target impedance. The value can be determined by the equation

$$Z_{target} = \frac{\mathrm{d}V}{\mathrm{d}I} \tag{1}$$

where dV represents the desired voltage ripple on the power rail and dI represents the maximum current change. The dV value is set to 5% of output voltage which is equal to 250 mV, and dI is equal to 10 A which then leads to target impedance value of 25 mΩ.

A group of different-value capacitors with low equivalent series resistance (ESR) is used to ensure that the PDN impedance value is below the target impedance. The purpose of capacitors with lower values is to control the impedance at higher frequencies and purpose of capacitors with larger capacitance is to control the impedance value at lower frequencies [5]. In this paper, six different capacitance values are used for covering frequency range as wide as possible. The total nominal capacitance is 255.3 µF.

The value of the output inductor ensures that the buck converter is always in the continuous conduction mode of operation. The selected value of the inductor is 1.5 µH [6].

Important part of designing output network of buck converter is the behavior of output voltage during load transient. The chosen value for undershoot and overshoot is 5% of the nominal output voltage which is equal to 250 mV. The following equations

$$C_{out} > \frac{L \cdot \mathrm{d}I^2}{2 \cdot V_{over} \cdot V_{out}} \tag{2}$$

$$C_{out} > \frac{L \cdot \mathrm{d}I^2}{2 \cdot V_{under} \cdot D \cdot (V_{in} - V_{out})} \tag{3}$$

which are given in [7], where C_{out} is the output capacitance, L is the inductance of an output inductor, dI the maximum current change, V_{over} the overshoot value, V_{out} the output voltage, V_{under} the undershoot value, D duty cycle and V_{in} is the input voltage give minimum capacitance value for the desired overshoot and undershoot

value. When the data from Table I is used the result is that the output capacitance needs to be larger than 95.4 µF.

TABLE I: Design parameters of a buck converter.

Parameter	Value
V_{in}	13.5 V
V_{out}	5 V
dI	10 A
L	1.5 µH
D	0.37

B. Buck converter LM61495Q1

LM61495Q1 10 A is a high power density buck converter with wide range of input voltage (3 -36 V) and adjustable output voltage which can be setup with the combination of resistors in the voltage feedback loop. The converter can have two behaviors while lightly loaded, when output current is smaller then 1/10 of the maximum output current. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior, called FPWM mode, maintains constant frequency even when unloaded. The mode can be selected on the pin *SYNC/MODE* pin [6]. The frequency is also adjustable, it can be set on the pin *RT* with a resistor or when connected to VCC for 400 kHz and connected to GND for 2.2 MHz. Spread spectrum is configurable using the *SPSP* pin. Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation [8].

C. Two-port shunt method

Two-port shunt method is used for measuring low-impedance structures such as PDN. The main advantage of using this method is that by using the two-port impedance measurements the effect of series connection discontinuities can be greatly reduced, which is the largest error contributor of one-port measurements [4]. Figure 1 shows measuring setup. The impedance can be calculated by the equation

$$Z_{DUT} = \frac{Z_{VNA}}{2} \cdot \frac{S_{21}}{1 - S_{21}} \tag{4}$$

while S_{21} is measured scattering parameter with the vector network analyzer (VNA).

D. Description of PCB

Layout of the four layer PCB is designed following the evaluation module board [9]. Stackup is shown in Table II. Wide and thick output plane is used to reduce the parasitic inductance and for better thermal performance of the buck converter. Ground vias are added beneath the converter for better thermal conductivity. The jumpers on the board are added to enable or disable converter, to switch the frequency (400 kHz or 2.2 MHz), to enable or disable spread spectrum and to choose the mode of operation (auto or FPWM). The board is designed to have three different

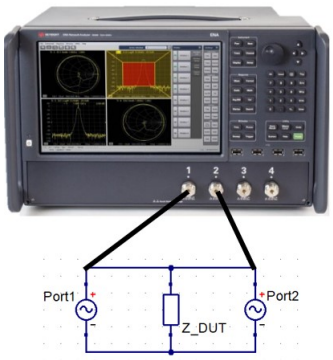


Fig. 1: Shunt method setup.

TABLE II: PCB layer stackup.

Name	Material	Type	Thickness
Top layer	Copper	Signal	70 µm
Dielectric 1	FR-4		100 µm
Inner layer 1	Copper	Ground plane	35 µm
Core	Core		1.2 mm
Inner layer 2	Copper	Signal	35 µm
Dielectric 2	FR-4		100 µm
Bottom layer 2	Copper	Signal	70 µm

versions of the output network, version A (Figure 2) that has all capacitors close to the IC, version B (Figure 3a) where all capacitors are placed close to the output and version C (Figure 3b) where the capacitors are again close to the output but some capacitors are removed leaving the total nominal capacitance of 179.5 µF.

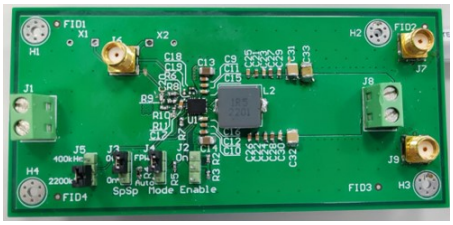
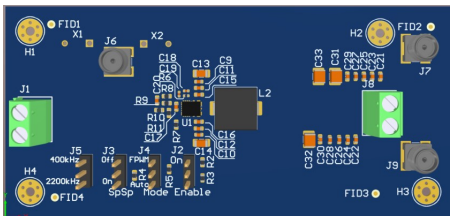


Fig. 2: Assembled printed circuit board - version A.

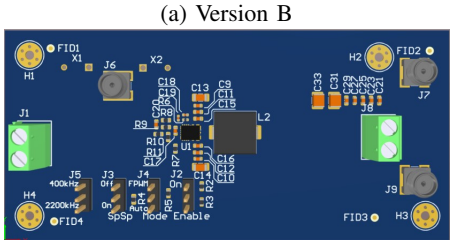
E. Simulation

Simulation process starts with SPICE simulation where the SPICE models of capacitors, available on the manufacturer's website [10], are added and scattering parameters are simulated in the shunt method configuration.

For a better estimate of the output network impedance, 3D electromagnetic simulations are performed using finite element method (FEM) solver. For this kind of simulations it is necessary to have the PCB layout and stackup with material parameters defined. The permittivity and dissipation factor of the core and prepreg materials are modeled by the frequency-depended Djordjevic-Sarkar model [11]. The mesh is adaptive at 100 MHz, while the sweep is interpolating with 100 points per decade (logarithmic scale) in the frequency range from 10 kHz to 100 MHz. Two circuit ports [12] are defined between the middle pin and the ground pin of the SMA connectors.



(a) Version B



(b) Version C

Fig. 3: Versions of output network shown in Altium Designer 3D viewer.

The differences between simulation types are shown in Figure 4. The main reason for such a difference between the simulations is that in SPICE simulation the parasitic elements of the PCB are not included.

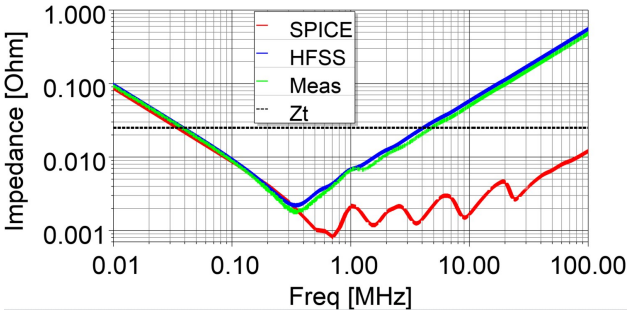


Fig. 4: Comparison of different simulation types and the measurement.

III. Results

A. Efficiency

The efficiency is defined as the ration of the output and input power commonly expressed in percentage. Table III shows the efficiency of three different cases of the output network.

TABLE III: Measured efficiency.

Case	V_{IN} [V]	I_{IN} [A]	V_{OUT} [V]	I_{OUT} [A]	Efficiency [%]
A	13.11	4.14	4.96	9.99	90.3
B	13.17	4.21	4.98	9.97	89.5
C	13.21	4.13	4.99	9.98	91.3

B. Comparison of simulation results and measurements in the frequency domain

The measurements are done using the shunt method at two SMA connectors that are placed on the PCB (J7 and J9), as shown in Figure 5. The PDN impedance is extracted from the measured scattering parameters. Figure 6 shows simulation and measurements results of output network impedance. It can be observed that cases A and B are matching at lower frequencies because they have the same capacitance, but they differ at high frequencies because of different parasitic inductance due to capacitors placement. The case C has lower capacitance and impedance characteristic is higher at lower frequencies. Table IV shows extracted values for capacitance at 10 kHz, equivalent series inductance (ESL) at 100 MHz and ESR extracted at the self-resonant frequency of each simulated and measured test case when buck converter in not powered.

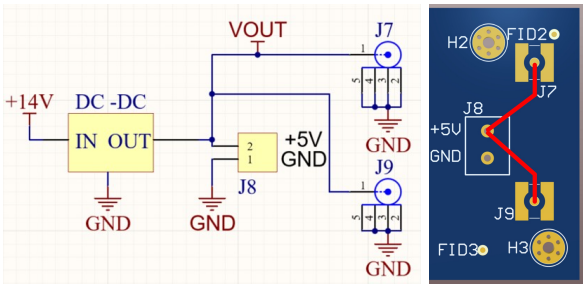
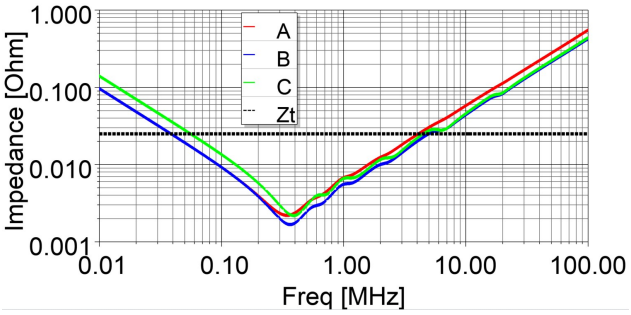
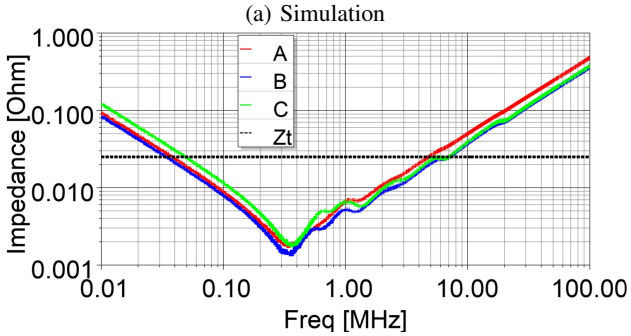


Fig. 5: Shunt method configuration: schematic (left), layout (right).



(a) Simulation



(b) Measurements

Fig. 6: Output impedance when the converter is off.

Figure 7 shows output impedance when the converter is turned on, off (without bias) and when the bias voltage is applied at the output connector. The red curve shows how the impedance characteristic is changed from blue when the bias voltage is applied, capacitance value is decreasing and the lower part of frequency characteristic is shifted to the right. At the high frequency there is no change

TABLE IV: Extracted values from simulation and measurements.

Case	A		B		C	
	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
C (10 kHz) [µF]	164	173	164	195	113	130
ESL (100 MHz) [pH]	879	765	675	570	700	592
ESR [mΩ]	1.8	2.2	1.3	1.7	1.8	2.2

due to the bias. Table V shows numerical values extracted from manufacturer's website, how capacitance is changed when the bias is applied [13]. The green curve on the graph shows the characteristic when the buck converter is turned on, output current is 5 A. The impact of the converter can be observed at lower frequencies. High frequency part depends on the total inductance of the output network (ESL, parasitic inductance of the plane, etc.). The characteristic with output current of 5 A does not differ from characteristic with output current 100 mA or 10 A.

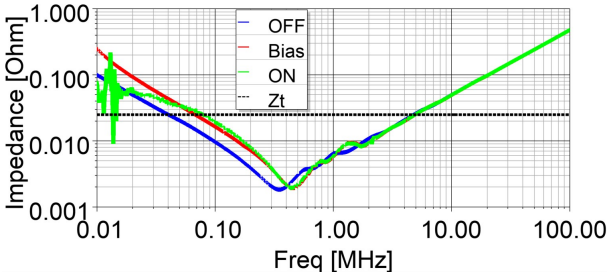


Fig. 7: Output impedance when the buck is turned on, off and with the bias voltage applied.

TABLE V: Capacitance change due to bias of 5 V

C [µF]	C bias [µF]	Qty.	∑ C [µF]	∑ C bias [µF]
100	46	1	100	46
47	26.8	2	94	53.58
22	5.5	2	44	11
4.7	2.8	3	14.1	8.32
1	0.73	3	3	2.19
0.1	0.096	2	0.2	0.192
			255.3	121.3

Figure 8 shows the impedance characteristic of three cases when the buck converter is turned on. As well as in the case when buck is turned off, cases A and B are different only at high frequencies due to different parasitic inductance, and the case C characteristic, with lower capacitance is shifted at lower frequencies.

C. Measurements in the transient domain

Transient response describes how a supply responds to a sudden change in load. That sudden change can cause large voltage transient undershoots and overshoots. Capacitors are used for maintaining stable voltage output, to provide short-term source of charge during the transient. Figure 9 shows the load transient response of the buck converter. Due to imperfection of the used active load device which has 3-A dip during transient from high to low level current, settings on the device is set from 10 A to 3 A to achieve the transient from 10 A to 0 A. All three cases have similar response, an overshoot of 300 mV. According to [14] current profiles have frequency content depending on duration and when that change is in microseconds it only depends on the VRM (Voltage Regulator Module) and not on the other parts of the PDN like capacitors, PCB planes, package and on-die capacitance.

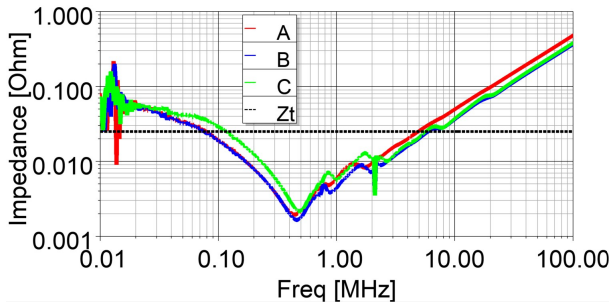


Fig. 8: Output impedance when the converter is on.

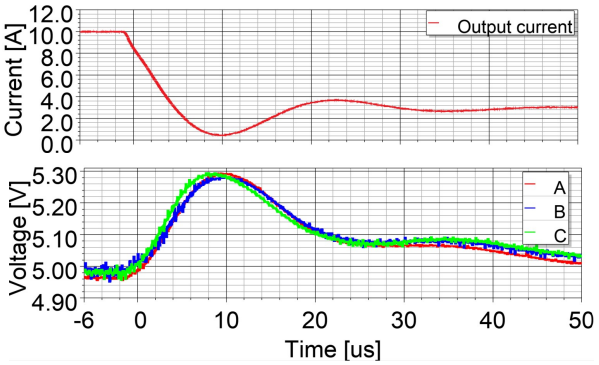


Fig. 9: Load transient.

IV. Conclusion

This paper shows design, simulation and measurements of the PDN. Simulations are done in the SPICE simulator and commercial EM solver. The most important factor in the design of the PDN is defining the target impedance. The 3D electromagnetic solver gives more realistic results than SPICE when compared to the measurements. The change of capacitance due to the applied bias voltage has to be considered during design. Load transient depends on the magnitude of the current change dI and on how fast that change is. If the change is in the range of microseconds then the voltage overshot is defined by the voltage regulator. Future work includes testing the device with faster load transients.

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