High Speed DPWM for Digital Power Converter Controller

Y. Smirnov*, V. Subotskaya*, M. Tulupov* and E. Bodano*

*Infineon Technologies AG, Villach, Austria
volha.subotskaya@infineon.com

Abstract - This study proposes a new architecture of digital pulse width modulator (DPWM) for power converter with digital control loop. The described architecture is based on a new counter-based concept. The new approach requires two counter loops: a slow big one and a fast small one. The fast counter loop is driven by a clock generated with a digital implemented ring oscillator, which is located on the chip close to the DPWM block. The slow counter measures the switching period. The fast counter provides the high precision duty cycle. The proposed concept was examined on the buck converter with 10-32V input voltage range, 5.8V output voltage, 2MHz switching frequency, 4.7uH filter inductance and 22uF filter capacitance. A proportional–integral–derivative (PID) controller was taken as a control loop feedback mechanism. To maintain the optimal duty cycle resolution of the DPWM the 576MHz ring oscillator was required. The proposed architecture improves the static characteristics of the converter while there is no impact on the dynamic characteristics. The results are showing that the output voltage ripple can be improved by 15% with absolute improvements of 14.4mV and the output current ripple can be reduced by 220mA for 1.1A load current. The ring oscillator frequency deviation of -20% to +30% has a small impact on the functional efficiency of the DPWM.

Keywords - switch-mode power conversion, digital control, digital pulse width modulation, high speed DPWM, SMPS

1. INTRODUCTION

Integrated DCDC converters are an important building block in power management, which should be highly efficient, fast to regulate the output voltage depending on the change of the external parameters and easily adjustable to accommodate the different external components [1]. Such requirements create a great interest in the digital-based approach of DCDC converter implementation.

Digital control for power dc-dc converters has significant advantages compared to analog architectures [2]. It introduces not only simple techniques for advance control [3], [4], but also it makes it possible to reuse the same hardware architecture for a different output power by simply changing the configuration value of the registers. From an integrated circuit design point of view digital flow enables the short development time, because it has automated tools and well-structured high-level verification methodology. Digital circuits also have significant benefits for technology transfer and can be tested on FPGA board without spending the effort on a dedicated test chip.

On the other hand, the digital control mode converters have also the disadvantages. One of the most common issues is connected with the digital pulse width modulator (DPWM), which forms duty cycle duration and has a direct impact on static characteristics of a dc-dc [5]. High resolution of PWM is required to decrease output voltage ripple and to avoid limit-cycle oscillation effect [6]. In order to solve this issue, different architectures were proposed. Most of the proposals are trying to achieve high resolution time quantization using a tapped string of delay cells, which is often called delay line [7]. Such circuits take advantage of the linear propagation, which is a function of a number of delay cells. The delay is controlled by the multiplexer driven by the n lowest bits of the duty cycle digital value [6]. This multiplexer and a big number of controlled delay cells is the drawback of this approach. The alternative solution is based on combination of the counter and delay line approach. In such systems most and least significant bits of duty cycle digital word are used to control counter- and delay-based parts respectively. The delay-line in this architecture type can be implemented from analog buffers [8] or from digital cells [9]. The main disadvantage of the analog buffers is to make the design stable over the process, voltage and temperature variations. One of the approaches to remove limit-cycle oscillation effect from the output voltage is to use DPWM based on second-order sigma-delta [9]. This concept requires separate computation units, which can introduce some additional total loop delay and as a result worsen the output dynamic characteristics of the dc-dc converter.

This paper presents the new digital high speed pulse width modulator approach developed for the buck converter based on two counters, one of which is slow and measures the switching period, the other which is fast and provides a high precision duty cycle. The proposed architecture improves the static characteristics of the converter while there is no impact on the dynamic characteristics.

The paper is organized as follows: the buck architecture is presented in section I, the high speed DPWM is described in Section II, the impact analyses on the static characteristic of the dc-dc is shown in Section III and Section IV summarizes the simulation results, and sets the tasks for future work.
II. DC-DC ARCHITECTURE

In Fig.1, a buck converter with digital control is shown. The buck converter consists of 4 blocks: analog filter, analog-to-digital converter, control unit, pulse width modulator.

A PWM output signal \( c[n] \) controls two switches, PMOS and NMOS. When \( c[n] \) is equal to 1, PMOS conducts and the current charges the inductor, and the output capacitor. When \( c[n] \) is equal to 0, NMOS conducts and the inductor discharges the current to the output capacitor. This repeats periodically with period \( T_s = 1/f_s \), where \( f_s \) is the converter switching frequency. The switching nature of the converter converts the DC input voltage to the desired output voltage which is defined as function of input voltage:

\[
V_{\text{out}} = DV_{\text{in}},
\]

where \( D \) is a fraction of time when PMOS is conducting and is called duty cycle.

The buck converter should regulate the output voltage in the specified window irrespective of the line or load changes in the defined region. The reaction time should be small enough to guarantee proper regulation. Therefore, the duty cycle \( D \) cannot be constant over all conditions. Thus, DCDC converter requires a smart control concept to manage both load and line changes. One of the common approaches is the proportional-integral-derivative compensator to generate the duty cycle of the command \( d[t] \). The simplified version of the compensator can be described using the following equations:

\[
\begin{align*}
    u_p[t] &= K_p e[t], \\
    u_i[t] &= u_i[t-1] + K_i T_e e[t] \\
    u_d[t] &= \frac{K_d}{T_s} (e[t] - e[t-1]) \\
    u[t] &= u_p[t] + u_i[t] + u_d[t]
\end{align*}
\]

where \( e[t] \) is the digital voltage error signal generated by ADC, which compares output voltage signal with predefined reference value. The gains \( K_p, K_i \) and \( K_d \) are designed so as to meet the control loop specifications, such as a crossover frequency, a phase margin and a switching frequency. It is important to notice that the compensator produces the computational delay, \( t_{\text{calc}} \), which is a part of total loop delay and has the impact on dynamic characteristics of dc-dc converter.

III. HIGH SPEED DIGITAL PULSE WIDTH MODULATOR

The buck converter with digital control uses a digital pulse width modulator as digital-to-analog converter. A discrete error of signal transformation depends directly on PWM resolution. If it is not high enough, output voltage ripple can be significant and limit-cycle oscillation effect appears. Limit-cycling oscillation occurs in the dc-dc system where the resolution of PWM is smaller than the resolution of the corresponding output voltage/feedback ADC. In general, a non-limit-cycling condition is described by the following equation:

\[
q_{\text{adc}} > V_{\text{dpwm}},
\]

where \( q_{\text{adc}} \) and \( q_{\text{dpwm}} \) are the last significant bits of the ADC and DPWM respectively. As one can see, DPWM resolution has a direct impact on the output ripple voltage.

In Fig.2 a block diagram of the proposed high speed DPWM is presented. It contains the two counters which are working at different frequencies. Counter 1 is driven by the system frequency of 72MHz. It is responsible for setting an output trigger at the beginning of every switching period. Counter 2 is more accurate. It does not work during the entire switching period, but only during the time when the output value of counter 1 is equal to the six highest bits of the duty cycle. For this purpose, the special enable signal is generated. Counter 2 is driven by a higher clock frequency of 576MHz. When the output value of counter 2 is equal to the last three significant bits of the duty cycle \( d[2:0] \), it generates a reset strobe for the output trigger.

A generalized behavior of the DPWM ramp is illustrated in the Fig. 3. From this figure it is clear that the resolution of the DPWM is defined by the resolution of the fast counter 2. The clock frequency for the second counter is generated by the ring oscillator, which is small and can be implemented using only digital cells. Despite the fact that the ring oscillator is not so precise, it is possible to achieve an accuracy of \( \pm 30\% \). It is quite a big variation, but it depends only on the temperature, which changes slowly and the PID core (illustrated in the Fig.1 PID core) has enough time to compensate this inaccuracy. Some advanced calibration techniques can also be used to decrease the generated clock variation range to \( \pm 1\% \).

The power consumption of the described converter should increase slightly, because only limited numbers of sub-blocks are driven by the high frequency: counter 2 and the driver finite state-machine. These sub-modules
occupy a small part of the design compared to the PID core. Increased power consumption can also be compensated in case the increased DPWM resolution is high enough to eliminate the noise-shaping block from the design. One of the advantages of the proposed solution is that the control unit can be tested by FPGA.

### TABLE I. BUCK PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>10-32V</td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>5.8V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>2MHz</td>
</tr>
<tr>
<td>Filter Inductance</td>
<td>4.7uH</td>
</tr>
<tr>
<td>Filter Capacitance</td>
<td>22uF</td>
</tr>
</tbody>
</table>

First of all, the frequency response was taken to prove that both systems are stable and can react similarly to the external disturbances. The Matlab function “Frestimate” was used for this purpose. The magnitudes and the phases of the frequency response can be observed in Fig. 4. Blue and red lines are converters with counter-based and high speed DPWMs respectively. The calculated bandwidth is about 100kHz and the phase margin is about 78°. As was expected from the frequency response analysis and was proven in simulations, the reaction on line and load disturbances for both types of controllers is the same and the difference is less than 1%.

The second test compares the output ripple of the converters for different input conditions. During the simulation load current and input voltage changes from 0.12A to 1.2A and from 10V to 32V respectively. Since the analog integrated clock circuit can have the variation of ±30% from the nominal values this was taken into the account in the test benches. In total 432 different input conditions were simulated for each type of DPWM. The output ripple was calculated as a difference between the highest and the lowest values of the output voltage or output current in the 2ms window in steady-state.

In Fig. 5a the results for the output voltage ripple are presented. Blue and orange lines correspond to the counter-based and high speed DPWM respectively. As can be seen the results are sorted by the counter-based ripple. From the plot it can be seen that the high speed DPWM gives lower ripple in all tested cases. The largest improvement achieved for the voltage ripple is about 14.4mV for an absolute value of voltage ripple about 50mV.

In Fig. 5b the results for the output current ripple are presented. Blue and orange lines correspond to the counter-based and high speed DPWM respectively. The results are sorted by the output voltage ripple values. It can be seen that it is possible to decrease output current ripple by about 220mA. The tendency shows that the high speed DPWM always provides lower ripple than the counter-based approach.

In Fig. 5c the data from Fig. 5a and Fig. 5b is combined on one plot, but results are normalized by the counter-based values. A blue line corresponds to counter-based DPWM and that is why it equals always 1. The orange and yellow lines are voltage and current ripple of the high speed DPWM respectively. This figure shows that the average ripple reduction is about 15%.

As was previously mentioned, the high speed DPWM requires a ring oscillator, which is temperature dependent. Thus, some tests were conducted to see what impact a ring oscillator has on the output ripple of the DPWM. In Table 2 the results of these tests are presented. The ring oscillator variation is about ±30% of the nominal frequency, which is 576MHz ± 173MHz. 16 different input conditions were checked for every deviation of the oscillator. In the second column the output ripple for the counter-based DPWM can be observed.

The test shows that the largest ripple reduction happens if the oscillator frequency has a zero or positive deviation: 576MHz, 633MHz, 691MHz and 748MHz. The
output ripple improvements for the negative deviation are not large, but still significant. The only cases that do not provide any benefits are located in the left low corner of the table. This can be explained by the fact that if DPWM frequency is getting lower, a larger error is introduced by every additional bit. This is illustrated in Fig. 6, which shows the influence of DPWM resolution on the output voltage ripple. It can be seen that the larger the DPWM resolution is, the lower the impact each additional bit has.

**Figure 5.** Simulation results for control-to-output magnitude and phase responses for the system with counter-based DPWM and for the system outcome of this research is that the optimal DPWM resolution is 8 bits, which requires 576 MHz ring oscillator with high speed DPWM.

**TABLE II.** Simulation results for voltage output ripple as function of ring oscillator variations

<table>
<thead>
<tr>
<th>DPWM frequency, MHz</th>
<th>72</th>
<th>403</th>
<th>460</th>
<th>518</th>
<th>576</th>
<th>633</th>
<th>691</th>
<th>748</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Test configurations</td>
<td>Counter-Based DPWM, mV</td>
<td>High speed DPWM, mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vin = 10V, Iload = 0.12A</td>
<td>17.6</td>
<td>15.6</td>
<td>15.0</td>
<td>15.1</td>
<td>14.7</td>
<td>14.8</td>
<td>14.7</td>
<td>15.1</td>
</tr>
<tr>
<td>Vin = 10V, Iload = 0.5A</td>
<td>17.4</td>
<td>15.1</td>
<td>14.3</td>
<td>14.8</td>
<td>14.4</td>
<td>14.1</td>
<td>14.4</td>
<td>14.6</td>
</tr>
<tr>
<td>Vin = 10V, Iload = 0.9A</td>
<td>16.8</td>
<td>14.7</td>
<td>14.1</td>
<td>14.1</td>
<td>13.5</td>
<td>13.8</td>
<td>14.1</td>
<td>14.0</td>
</tr>
<tr>
<td>Vin = 10V, Iload = 1.2A</td>
<td>16.9</td>
<td>14.3</td>
<td>14.3</td>
<td>14.1</td>
<td>13.2</td>
<td>13.6</td>
<td>13.6</td>
<td>13.8</td>
</tr>
<tr>
<td>Vin = 18V, Iload = 0.12A</td>
<td>29.3</td>
<td>23.6</td>
<td>23.7</td>
<td>23.2</td>
<td>22.5</td>
<td>22.9</td>
<td>22.9</td>
<td>23.1</td>
</tr>
<tr>
<td>Vin = 18V, Iload = 0.5A</td>
<td>29.2</td>
<td>23.7</td>
<td>27.0</td>
<td>23.5</td>
<td>22.7</td>
<td>23.1</td>
<td>23.2</td>
<td>23.2</td>
</tr>
<tr>
<td>Vin = 18V, Iload = 0.9A</td>
<td>29.4</td>
<td>24.3</td>
<td>23.9</td>
<td>23.6</td>
<td>23.4</td>
<td>23.2</td>
<td>23.5</td>
<td>23.4</td>
</tr>
<tr>
<td>Vin = 18V, Iload = 1.2A</td>
<td>29.1</td>
<td>25.0</td>
<td>24.3</td>
<td>24.4</td>
<td>23.9</td>
<td>23.8</td>
<td>24.2</td>
<td>24.3</td>
</tr>
<tr>
<td>Vin = 25V, Iload = 0.12A</td>
<td>33.6</td>
<td>33.8</td>
<td>25.9</td>
<td>26.0</td>
<td>25.3</td>
<td>25.2</td>
<td>25.6</td>
<td>25.9</td>
</tr>
<tr>
<td>Vin = 25V, Iload = 0.5A</td>
<td>34.6</td>
<td>32.3</td>
<td>30.4</td>
<td>26.8</td>
<td>26.2</td>
<td>26.6</td>
<td>26.4</td>
<td>26.9</td>
</tr>
<tr>
<td>Vin = 25V, Iload = 0.9A</td>
<td>34.5</td>
<td>34.5</td>
<td>33.3</td>
<td>28.3</td>
<td>26.7</td>
<td>27.5</td>
<td>27.4</td>
<td>27.2</td>
</tr>
<tr>
<td>Vin = 25V, Iload = 1.2A</td>
<td>33.6</td>
<td>30.6</td>
<td>32.6</td>
<td>27.3</td>
<td>26.4</td>
<td>26.4</td>
<td>27.2</td>
<td>27.3</td>
</tr>
<tr>
<td>Vin = 32V, Iload = 0.12A</td>
<td>38.1</td>
<td>30.1</td>
<td>28.3</td>
<td>28.5</td>
<td>27.5</td>
<td>27.4</td>
<td>28.1</td>
<td>28.3</td>
</tr>
<tr>
<td>Vin = 32V, Iload = 0.5A</td>
<td>38.2</td>
<td>42.9</td>
<td>35.8</td>
<td>31.7</td>
<td>28.5</td>
<td>29.5</td>
<td>28.4</td>
<td>29.1</td>
</tr>
<tr>
<td>Vin = 32V, Iload = 0.9A</td>
<td>38.4</td>
<td>35.8</td>
<td>32.6</td>
<td>30.9</td>
<td>29.3</td>
<td>30.3</td>
<td>29.4</td>
<td>29.7</td>
</tr>
<tr>
<td>Vin = 32V, Iload = 1.2A</td>
<td>36.0</td>
<td>30.7</td>
<td>30.0</td>
<td>30.0</td>
<td>29.1</td>
<td>29.1</td>
<td>29.6</td>
<td>30.1</td>
</tr>
</tbody>
</table>
V. CONCLUSION

This paper proposes a new architecture for a digital pulse width modulator. The new high speed DPWM consists of two basic blocks: slow and fast counters. The slow counter is responsible for keeping the switching period constant, and the fast counter makes the duty cycle more precise. This concept also requires a high frequency ring oscillator to drive the fast counter. The power consumption is slightly increased because only a small part of the design is driven by this high frequency.

In order to evaluate the impact of this approach the high speed DPWM was tested as a part of a buck converter and its results were compared with the counter-based DPWM converter. Based on the results it is possible to confirm that the high speed DPWM can decrease both output voltage and current ripples by about 15%, with maximum absolute improvements of about 15mV for the voltage ripple and about 220mA for the current ripple. It is also important to notice that the high speed DPWM has the same frequency response as a standard counter-based approach. This means it does not increase reaction time for different kind of line and load jumps. Furthermore, it was shown that the proposed solution is quite stable to frequency variation. It shows stable improvements if the DPWM frequency changes in the range -20% to +30%. Another observation shows that the higher DPWM frequency becomes, lower the impact of each additional bit. The simulation results show that the optimal DPWM resolution for this particular buck converter is 8bits. There is no sense in making it higher because it does not provide any benefits to the output ripple.

The study of this problem is relevant and important for the development of power dc-dc converters, especially if the tolerances for the output ripple are tight and the old implementation approach cannot guarantee the performance. The future step of the project is to make FPGA prototype in order to prove the concept and to evaluate the power consumption increase of the proposed DPWM architecture.

REFERENCES