Measurement Setup for Characterizing Immunity of Integrated Circuits to Pulsed Electric Fields using the IC Stripline

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***Abstract* - A measurement setup is presented for characterizing the immunity of an ambient light sensor (ALS) integrated circuit (IC) to pulsed electric fields for consumer electronics products. The charge transferred to the photodiode during the rising and falling edges of the pulses is integrated and processed by the sensor, and it generates a shift in the ALS reading mean value. The pulsed electric fields up to 50 kV/m are applied to the IC using an open-terminated IC stripline with a septum height of 1.5 mm above the IC that is driven by voltage pulses with positive and negative amplitudes up to 80 V. The circuit for generating the voltage pulses synchronized with the on-chip photodiode integration phase is presented, and the achieved rising and falling edge characteristics are measured. The ALS reading shift is measured as a function of the voltage pulse amplitude, DUT orientation, level of illumination, and integrator gain. The relationship between the ALS reading shift and the electric field amplitude is established as a figure-of-merit for the immunity of the IC to pulsed electric fields.**

Keywords - pulsed electric field immunity; IC stripline; electromagnetic compatibility; ambient light sensors; charge injection

I. INTRODUCTION

The scope of electromagnetic compatibility testing continuously increases with the number of integrated circuits and the complexity of consumer electronics products. A subset of EMC tests are the radiated immunity measurements [1]. The radiated immunity of complex systems, such as electrical/electronic subassemblies (ESA) at the vehicle level [2], can be validated by testing each component separately [3].

At the level of individual ICs, such as integrated voltage-controlled oscillator (VCO) circuits [4], the radiated immunity is characterized according to the IEC standard 62132-8 [1] using the IC stripline, a component that enables applying electric and magnetic fields in the radio-frequency (RF) band to the device-under-test (DUT) through capacitive and inductive coupling [5].

Various types of open and closed IC striplines are designed and modelled in literature in order to achieve good load matching, i.e. having the voltage standing wave ratio (VSWR) below 1.25 in the frequency range up to 4 GHz [4], [5], [6]. The influence of the IC package on the EM field distribution inside the stripline is also considered when designing the IC stripline [7], [8].

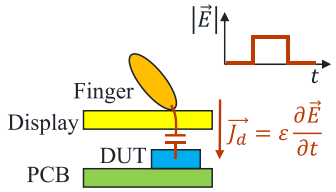


Figure 1: A consumer electronics application example motivating the pulsed electric field (*E*-field) testing requirement for ICs.

Ambient light sensors (ALS) are ICs that use a photodiode (PD) for generating a photo-current in the presence of visible light. The photo-current is converted into a digital value proportional to the illumination intensity using an on-chip current integrator and an analogue-to-digital converter (ADC).

Figure 1 presents an ALS application in a consumer electronics product. The finger touching the display is capacitively coupled to the DUT inside the product. When the charged finger presses onto the display, a pulsed electric field E is generated. During the rising and falling edges of the pulse, a non-zero displacement current J_d flows into the photodiode area of the sensor, equivalently to a photo-current, and it generates an erroneous ALS reading. In addition to this example, pulsed *E*-fields may also originate from the display operation itself.

In this paper, an experimental setup for the characterization of the immunity of ICs to pulsed electric fields (*E*-fields) using the closed IC stripline is presented. The IC stripline is chosen because it enables defining the precise distance between the DUT and the metal plate that applies the *E*-field pulses. In contrast to the 50 Ω termination required by the IEC standard [1], the IC stripline is open-terminated in order to reduce the DC current requirements and the magnetic field component within the IC stripline cavity.

The paper is organized as follows. Section II presents the pulsed *E*-field immunity measurement setup, including the voltage pulse generator circuit, the pulse edge characteristics, and the setup noise characteristics. Section III presents the measurement results of an industrial ambient light sensor over several illumination levels, device orientations, and device settings. The results are discussed in Section IV, and Section V concludes the paper.

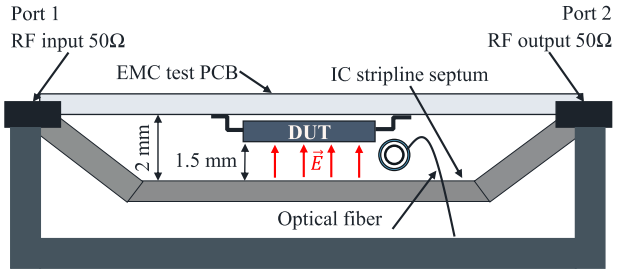


Figure 2: Cross-section of the closed IC stripline with a sidewall optical fiber input for controlling the illumination level within the cavity.

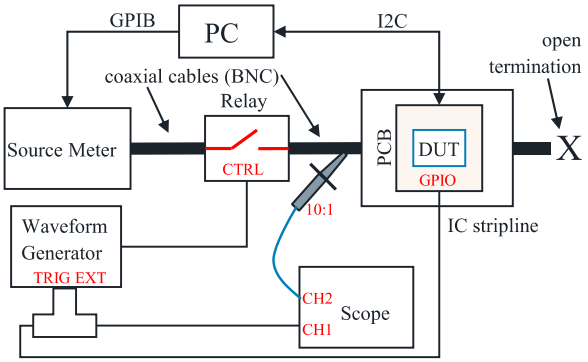


Figure 3: Block diagram of the pulsed *E*-field immunity measurement setup. Port 2 of the IC stripline is terminated in open circuit.

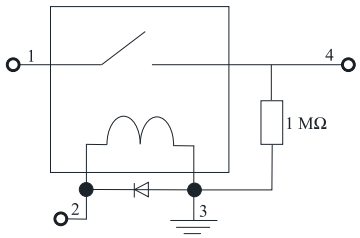


Figure 4: The schematic of the relay circuit. The Coto 9012-05-10 relay [9] connects the input pin 1 to the output pin 4 based on the control voltage applied across pin 2 and pin 3. The freewheeling diode between pin 2 and pin 3 protects the circuit against negative control voltage transients. The output (pin 4) has a weak pull-down resistor of 1 MΩ that defines the output voltage in the open circuit condition.

II. Measurement Setup

A. IC stripline for pulsed E-field immunity measurements

Figure 2 presents the cross-section of the closed IC stripline that generates pulsed *E*-fields from the septum that is 1.5 mm away from the DUT, which is soldered on the bottom layer of the 105 mm by 105 mm EMC test PCB on FR4 substrate. In this way, the distance of 1.5 mm between the DUT and the septum is precisely defined. Four DUT orientations relative to the septum are achieved by rotating the EMC test PCB. The setup is placed in a dark ambient, and the DUT is illuminated using an LED light source connected to the sidewall input by optical fiber. The illumination level is controlled by the LED current I_{LED}.

The *E*-field is uniform in the region between the septum and the ground plane, and the field strength is defined by the ratio of the voltage applied to the septum and the distance from the septum to the ground plane below the DUT [7]. Since the DUT size is comparable to the septum

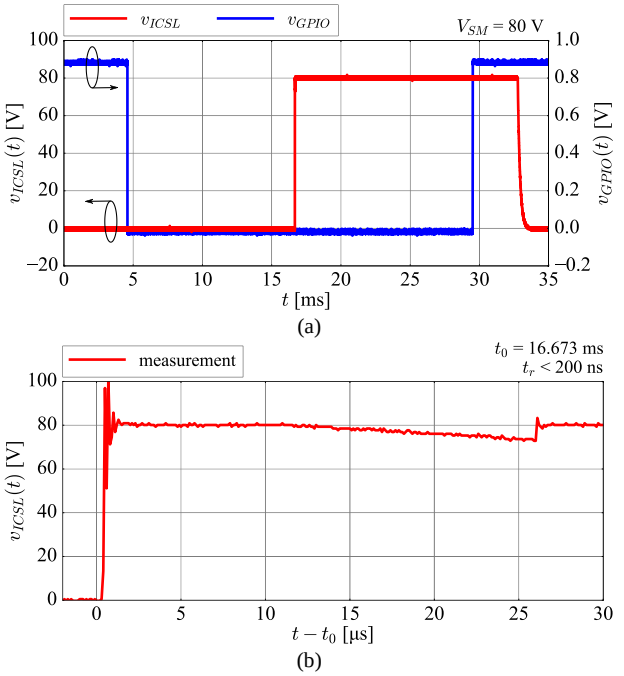


Figure 5: Rising voltage pulse edge: (a) timing relationship between the GPIO signal from the DUT (blue) and the signal applied to the IC stripline input (red), (b) zoom-in detail of the rising edge with the rise-time t_r under 200 ns. The additional voltage pulse at 27 µs is attributed to reflections due to the mechanical characteristics of the relay.

distance, the *E*-field is calculated using the 1.5 mm distance between the septum and the DUT surface, i.e. the active area of the IC that includes the ground plane. Therefore, a pulsed *E*-field amplitude of 50 kV/m is generated by applying a pulsed voltage amplitude of 75 V into the RF input of the IC stripline (Port 1 in Figure 2). Since most arbitrary waveform generators cannot generate voltages above 20 V, the voltage pulses are generated using the measurement setup presented in Figure 3.

The source meter (SM) that can generate DC voltages up to 100 V is connected to the IC stripline input by coaxial cables through the relay circuit shown in Figure 4. When the relay is closed, the IC stripline input voltage (pin 4 in Figure 4) is equal to the SM output voltage V_{SM} (pin 1 in Figure 4). When the relay is open, the 1 MΩ resistor pulls the IC stripline input voltage to 0 V. In this way, the relay circuit enables generating rising and falling voltage pulse edges with large amplitudes at the IC stripline input (port 2 in Figure 2) using low-voltage control signals applied to the relay control input (pin 2 in Figure 4).

If the IC stripline output (port 2 in Figure 2) would be terminated in 50 Ω according to [1], the maximum current flowing through the relay at SM output set to 80 V would exceed 1.5 A, which is above the maximum relay carry current of 0.5 A [9], thus destroying the relay. The IC stripline output port is therefore terminated in open circuit.

In order to synchronize the voltage pulse edges with the on-chip ALS integration, the relay control input is driven by a waveform generator that is externally triggered by the DUT signal (GPIO in Figure 3), which indicates that ALS integration is active. Figure 5 presents the rising voltage pulse edge measured using an oscilloscope, with channel 1 monitoring the GPIO trigger signal and channel 2 probing

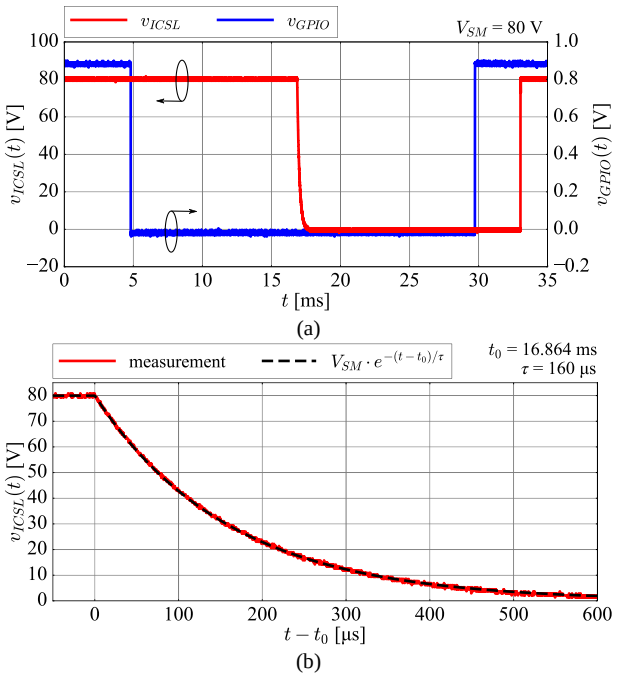


Figure 6: Falling voltage pulse edge: (a) timing relationship between the GPIO signal from the DUT (blue) and the signal applied to the IC stripline input (red), (b) zoom-in detail of the falling edge with the first order exponential shape defined by the time constant τ of 160 µs, resulting in a fall-time t_f of 352 µs.

the relay circuit output using a 10:1 probe. The rise time t_r is below 200 ns, with additional reflections due to the relay mechanical characteristics observed after 27 µs. Figure 6 presents the measured falling voltage pulse edge. The time constant τ of 160 µs is defined by the 1 MΩ pull-down resistance and the equivalent capacitance of 160 pF seen at pin 4 in Figure 4 when the relay is in the open position. Since the DUT responds to the total integrated displacement current, its output is not sensitive to the exact current profile. It was therefore decided to keep the 1 MΩ pull-down resistor regardless of the slow fall-time.

B. *Measurement setup noise floor*

The noise floor of the measurement setup is divided into two components: the ALS circuit noise, and the LED light source noise. The overall noise level is characterized by measuring a long time-series of ALS readings (expressed in "least significant bits", LSB) without any pulsed *E*-field applied. Figure 7a presents a time-series of 1000 samples measured at the LED light source current I_{LED} of 1 mA. The data are sorted into a histogram shown in Figure 7b with 20 bins. A normal distribution probability density function (PDF) is fitted onto the histogram, and the standard deviation σ of 25.4 LSB is extracted.

Table 1 presents the overview of the normal distribution parameters, i.e. mean value μ and standard deviation σ, obtained in this way over several illumination levels, two perpendicular device orientations on the IC stripline, and two device analogue gain (AGAIN) settings. The mean values under 90 degree orientation are higher than in the 0 degree case for the same LED current because the optical fiber illuminates the ALS photodiode under a different incident angle. The standard deviation of 8 LSB observed at 0 mA is attributed to the ALS circuit noise. The additional increase of the standard deviation with the light

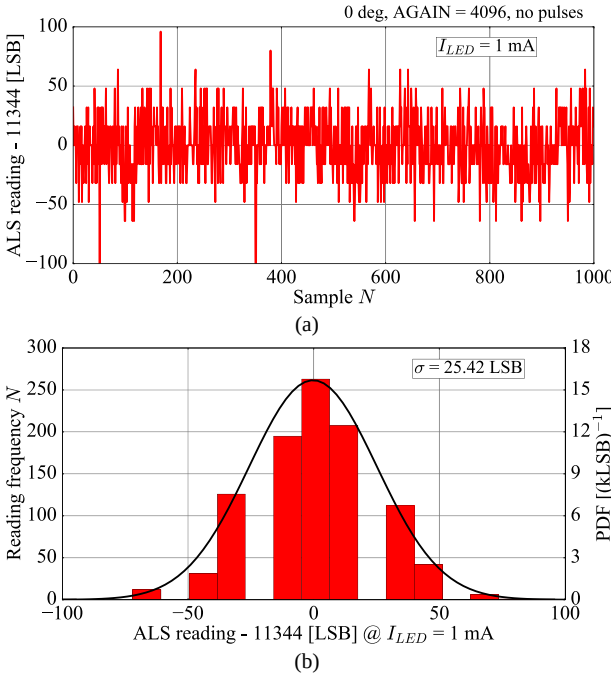


Figure 7: (a) Consecutive ALS reading samples under the illumination corresponding to LED current of 1 mA in the 0 degree orientation, (b) histogram of the sample reading frequency sorted into 20 bins with the fitted probability density function (PDF). The extracted standard deviation σ is 25.42 LSB.

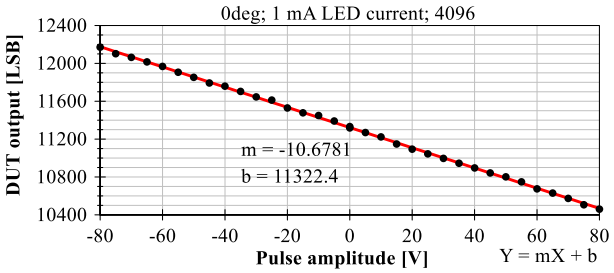
TABLE 1: MEAN VALUE μ AND STANDARD DEVIATION σ OF A 1000 SAMPLE LONG TIME-SERIES UNDER SEVERAL ILLUMINATION LEVELS, TWO PERPENDICULAR DEVICE ORIENTATIONS, AND TWO DEVICE ANALOGUE GAIN (AGAIN) VALUES.

AGAIN	I_{LED} [mA]	orientation [deg]	μ [LSB]	σ [LSB]
4096	0.0	0	0	8.16
		90	0	8.08
	0.2	0	355	11.15
		90	640	18.42
	0.5	0	4116	22.27
		90	7812	32.26
	1.0	0	11344	25.42
		90	21287	43.50
512	1.0	0	5886	10.55

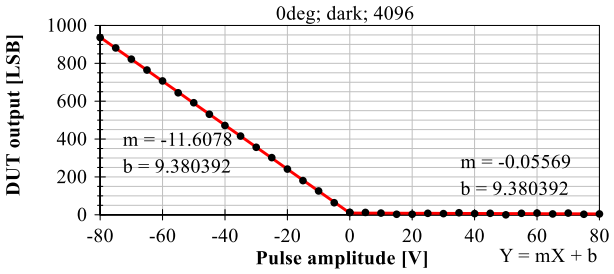
level is attributed to the LED light source noise, and it is within 35 LSB in the full range of illumination levels.

When the AGAIN setting is reduced from 4096 to 512, the ALS reading under the same illumination level decreases both in mean value and in standard deviation.

The noise floor characteristics of the measurement setup with the particular DUT presented in Table 1 are used as the baseline for determining the required averaging factor for the pulsed *E*-field immunity measurements as a function of the voltage pulse amplitude. Reducing the averaging factor from 1000 samples down to 10 samples significantly reduces the measurement time per pulse amplitude, while the achieved standard deviation remains within the same range as in Table 1. No significant increase in the standard deviation is observed when the voltage pulses are applied to the IC stripline input.



(a)



(b)

Figure 8: ALS reading (DUT output) measured as a function of the voltage pulse amplitude (black dots) and the interpolated function (red lines), taken in two illumination conditions: (a) LED current I_{LED} of 1 mA, (b) dark condition. The slope *m* and offset *b* are extracted separately for each piecewise linear part of the measured DUT output. The DUT analogue gain is set to 4096.

III. Experimental Results

The measurement setup introduced and characterized in Section II enables applying pulsed *E*-fields with both positive and negative pulse edges, which are synchronized with the on-chip ALS integration. The ALS reading in LSB is measured as a function of the voltage pulse amplitude in the range from -80 V (i.e. falling edge from 80 V to 0 V shown in Figure 6) to +80 V (i.e. rising edge from 0 V to 80 V shown in Figure 5) with a voltage step-size of 5 V.

Figure 8 presents the measurement results at two illumination levels. In Figure 8a, the LED current I_{LED} is set to 1 mA. The ALS reading at 0 V represents the undisturbed DUT output with the *E*-field pulse amplitude set to zero, which is equivalent to having no *E*-field pulses applied. The observed undisturbed ALS reading of 11322 LSB in Figure 8 is consistent with the value of 11344 LSB observed in the noise floor measurements in the same illumination condition given in Figure 7.

The ALS reading is observed to have a linear change with the voltage pulse amplitude, therefore the measurement data are interpolated according to the linear equation $Y = mX + b$, where X is the pulse amplitude (x-axis in Figure 8) and Y is the ALS reading (y-axis in Figure 8). The slope m of -10.7 LSB/V is the main pulsed *E*-field immunity characteristic of the DUT, and the offset b defines the corresponding DUT illumination level. The maximum observed absolute ALS error is 850 LSB.

The data in Figure 8a show that the difference in the rise time t_r and fall time t_f of the voltage pulses presented in Section II-A does not affect the slope m in the negative pulse amplitudes compared to the positive amplitudes.

In Figure 8b, the DUT is in the dark ambient, with the undisturbed ALS reading of 9 LSB. A linear relationship between the DUT output and the pulse amplitude is observed for negative pulse amplitudes, however at positive pulse amplitudes the ALS reading is clipped into the noise floor of 9 LSB, because the DUT does not support negative ALS values. The slope m and offset b are extracted separately for each piecewise linear part of the measured DUT output, and the maximum observed ALS output error is 925 LSB. The extracted slope m of -11.6 LSB/V at negative pulse amplitudes is in a similar range as in the illuminated case in Figure 8a.

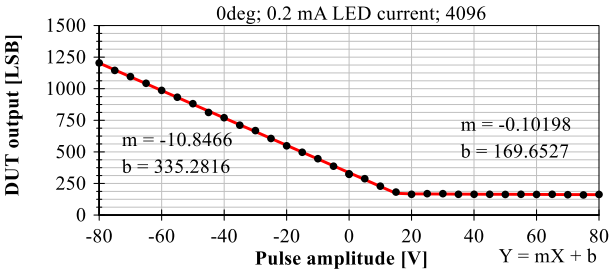


Figure 9: ALS reading (DUT output) measured as a function of the voltage pulse amplitude (black dots) and the interpolated function (red line), taken at LED current I_{LED} of 0.2 mA. The level at which the ALS reading is clipped increases with the illumination level. The DUT analogue gain is set to 4096.

TABLE 2: OVERVIEW OF THE INTERPOLATED SLOPE *m* AND OFFSET *b* UNDER SEVERAL ILLUMINATION LEVELS, TWO PERPENDICULAR DEVICE ORIENTATIONS, AND TWO DEVICE ANALOGUE GAIN (AGAIN) VALUES.

AGAIN	I_{LED} [mA]	orientation [deg]	*m* [LSB/V]	*b* [LSB]
4096	0.0	0	-11.61	9.4
		90	-11.61	8.4
	0.2	0	-10.85	335.3
		90	-10.98	627.4
	0.5	0	-11.87	4199.1
		90	-11.03	7803.7
	1.0	0	-10.68	11322.4
		90	-10.96	21232.7
512	1.0	0	-3.04	3126.3
		90	-3.04	5877.2

Figure 9 presents the measurement data with the LED current set to 0.2 mA, i.e. a medium illumination level. These measurement data show that the level at which the ALS reading is clipped is not always equal to 0 LSB, but rather it increases with the ambient illumination level. This behaviour is attributed to the ALS circuit operation.

Table I presents the extracted slope m and offset b over the following measurement conditions in the non-clipped part of the measurement data: two perpendicular device orientations, several LED current (I_{LED}) values, and two analogue gain (AGAIN) settings. All other DUT configuration settings are kept constant.

The slope m is approximately equal to -11 LSB/V across a wide range of illumination levels with AGAIN set to 4096. Reducing the AGAIN from 4096 to 512 under the same illumination level reduces the slope m down to -3 LSB/V, i.e. by a similar factor as AGAIN.

IV. Discussion

The presented measurement setup for characterizing the pulsed *E*-field immunity of ICs uses relay switching to enable generating voltage pulse amplitudes higher than what can be achieved by most arbitrary waveform generators. The drawback of the presented methodology is that the rising and falling edges have slow and widely different rise- and fall-times. The presented measurement data show that the extracted slopes *m* are not highly sensitive to the exact rise- and fall-times of the voltage pulses. This is explained by the implementation of the ALS function, which is based on integration of the displacement current flowing through the photodiode, rather than the exact profile of the current over time. The setup is therefore considered appropriate for measuring this family of ambient light sensors.

The mean values μ in Table 1 of the long time-series measurements taken without *E*-field pulses are consistent with the extracted offset values *b* in Table 2, which correspond to the ALS output values at 0 V voltage pulse amplitude, i.e. the undisturbed DUT output. This demonstrates the stability of the measurement setup and the repeatability of the measurements.

The measured noise floor of the measurement setup is within 44 LSB in the ambient illumination corresponding to the undisturbed DUT output of 21230 LSB, or 0.2%. This noise level is considered to be sufficient for extracting stable and accurate values of the slope *m*.

The unit of the slope *m* in this paper (LSB/V) is specific to a particular distance between the DUT and the IC stripline septum. A more general unit of measure would be expressed as LSB per kV/m of the *E*-field amplitude. The presented value of *m* equal to -11 LSB/V at 1.5 mm septum distance is equivalent to -16.5 LSB/(kV/m). In practice, the septum distance can be considered constant for a particular lab setup, therefore using LSB/V as the unit is appropriate during the characterization phase. The conversion to the more general unit of LSB/(kV/m) can be done as a final step in the pulsed *E*-field immunity report.

The negative sign of the measured slope *m* presented in Table 2, as well as the ALS error clipping effects observed in Figure 8b and Figure 9, indicate that the device is more sensitive to falling edges of the voltage pulse than the rising edges depending on the ambient illumination level. The data also indicate that the slope *m* reduces proportionally to the device analogue gain setting. This information about the IC characteristics are a useful input for defining the EMC mitigation strategies on the level of the consumer electronics product during the design-in phase of product development.

V. Conclusion

A measurement setup for characterizing the immunity of integrated circuits to pulsed electric fields based on the open-terminated IC stripline is presented. The circuit for generating voltage pulses with amplitudes up to 80 V is presented, with rise-times below 200 ns and fall times of 352 µs. The voltage pulse rising and falling edges are synchronized with the on-chip timing. The noise floor of the measurement setup is characterized, and it is divided into the on-chip analogue noise and the light source noise components. The relationship between the ALS reading error and the voltage pulse amplitude is measured over several illumination conditions, device orientations, and device analogue gain settings.

Acknowledgment

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References

[1] Integrated Circuits - Measurement of Electromagnetic Immunity - Part 8: Measurement of radiated immunity - IC stripline method, Int. Electrotechn. Commission, Geneva, Switzerland, IEC Standard 62132-8, 2012.

[2] Proposal for a new 06 series of amendments to UN Regulation No. 10 (Electromagnetic compatibility), Retreived: February 1, 2023, from https://unece.org/DAM/trans/doc/2019/wp29/ECE-TRANS-WP29-2019-020e.pdf.

[3] N. F. Bedjiah, M. Klingler, M. Kadi and R. Rossi, "Methodology to Validate the Radiated Immunity of Very Complex Systems by a Succession of Simple Component Radiated Immunity Tests at System Level," 2022 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), Spokane, WA, USA, 2022, pp. 561-564.

[4] J. Hwang, Y. Han, H. Park, W. Nah and S. Kim, "Radiated electromagnetic immunity analysis of VCO using IC stripline method," 2015 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Edinburgh, UK, 2015, pp. 147-151.

[5] H. Kang, W. Jung, K. Kim, H. H. Park and S. Kim, "Equivalent circuit model of the IC-Stripline coupling to IC package," 2014 IEEE 18th Workshop on Signal and Power Integrity (SPI), Ghent, Belgium, 2014, pp. 1-4.

[6] T. Mandic, R. Gillon, B. Nauwelaers and A. Baric, "Design and modelling of IC-Stripline having improved VSWR performance," 2011 8th Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Dubrovnik, Croatia, 2011, pp. 82-87.

[7] F. Fiori and M. Perotti, "On the use of the IC stripline to evaluate the susceptibility to EMI of small integrated circuits," 2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE, Wroclaw, Poland, 2016, pp. 306-309.

[8] M. Koohestani, M. Ramdani and R. Perdriau, "Impact of Mode Propagation on Radiated Immunity Characterization in Commonly Used TEM Cells," 2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Hangzhou, China, 2019, pp. 5-7.

[9] 9011, 9012 & 9117 miniature SIP Relays - Coto Technology, Retreived: January 20, 2023, from https://www.cotorelay.com/wp-content/uploads/2014/09/9011_series_reed_relay_datasheet.pdf.