Electrical Characterization of SiGeSn/Ge/GeSn-pin-Heterodiodes at Low Temperatures

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Abstract - The combination of the ternary alloy $Si_xGe_{1-x-y}Sn_y$ with $Ge_{1-y}Sn_y$ is very promising for electrooptical applications in the near infrared regime up to 2.5 µm wavelength. With the tunable bandgap at a non-varying lattice constant $Si_xGe_{1-x-y}Sn_y$ is predestined for the lattice matched growth on a Ge virtual substrate and the integration of pseudomorphic $Ge_{1-y}Sn_y$ layers with high Sn content (> 10 %). The main challenge of the growth of such alloys is to achieve a low density of defects. However, in the last few years there was a major progress in growing highly doped $Si_xGe_{1-x-y}Sn_y$ layers with good crystal quality. In this work we investigate the electrical characteristics of a $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$ -pin-heterodiode in a temperature range from 300 K to 8 K. This temperature depended measurement provides the opportunity for a more precise characterization of such diodes. A linear relation between reciprocal temperature and the ideality factor is found. With the extrapolation of this relation up to room temperature the ideality factor of the diode is calculated ($\eta = 1.22$). From the temperature dependent reverse current the activation energy is determined ($E_A = 0.178$ eV). We discuss the possibility to utilize such diodes for near infrared electro-optical applications.

Keywords – SiGeSn, Heterodiode, Electrical Characterization, Low Temperature,

I. INTRODUCTION

For the past decades, there has been a keen interest for integrating near-infrared (NIR) detectors and emitters on a Si-platform for lab-on-chip applications and on-chip / inter-chip communication [1]. The use of materials, which are compatible with Complementary-Metal-Oxid-Semiconductor technology, is essential for low-cost and high-volume fabrication.

The integration of Ge pin-diodes on a Si-platform is a popular technology for detector applications in the NIR wavelength regime [2]. Due to the smaller direct bandgap of Ge with respect to Si the efficient detection of wavelengths up to 1.6 µm is possible. At the same time, this bandgap limits the Ge pin detectors. While group III-V semiconductors can achieve much smaller bandgaps, the existing approaches for integration of such detectors on the Si-platform is complex [3]. Easily integrable solutions such as Schottky-barrier photodiodes are investigated, but cannot yet compete with Ge pin diodes due to their low internal quantum efficiency [4].

$Ge_{1-y}Sn_y$ alloys are a promising material system, to enable group IV pin diode detectors exceeding the range of applications beyond 1.6 µm. The incorporation of Sn, with its negative direct bandgap, into Ge leads to a decrease of the bandgap [5]. Depending on composition and strain, bandgaps corresponding to a wavelength of 2.5 µm at Sn concentrations of 11 % have already been demonstrated [6].

Additionally, with increasing Sn concentration in relaxed grown $Ge_{1-y}Sn_y$ layers the direct bandgap decreases faster than the indirect bandgap leading to a direct material. The transition from an indirect to a direct material is predicted for a Sn concentration in the range from 6.5 % to 11 % [7, 8]. However, the relaxation process is related to the formation of threading dislocations, making the layer inefficient for photonic applications. Thus, the incorporation of a pseudomorphic $Ge_{1-y}Sn_y$ layer with good crystal quality is preferred. This can be achieved by growing quantum well (QW) structures using a Ge virtual substrate (VS) and a lattice matched $Si_xGe_{1-x-y}Sn_y$ layer on a Si substrate. The incorporation of Si into $Si_xGe_{1-x-y}Sn_y$ leads to a higher bandgap at the same lattice constant. Therefore, the cladding layers are transparent for photons in the wavelength regime of the QW. With such devices it could be possible to detect as well as emit light in the NIR region beyond 1.6 µm. To assess the potential of these alloys it is necessary to characterize potential devices optically as well as electrically.

In this work, we present the electrical characterization of a $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$ -pin-heterostructure. High resolution X-ray diffraction (HR-XRD) measurements are taken to examine the crystal quality of the heterostructure as well es the Sn concentration of the QW. To obtain the temperature-dependent ideality factor of the pin-heterostructure, current-voltage sweeps were performed in a temperature range from 300 K to 8 K. To determine the activation energy the reverse current at -1 V is evaluated.

II. EXPERIMENTAL DETAILS

A. MBE Growth

The $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$ -separate confinement heterostructure (SCH) was grown in a 6”-MBE-System on a (100) Si-substrate as schematically depicted in Fig. 1. After building an ultra-thin Ge VS [9], the active layer stack was grown. The bottom layer of the stack is a 400 nm B doped $Si_{0.367}Ge_{0.533}Sn_{0.1}$ layer with an acceptor concentration $N_A = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$. The intrinsic region consists of a 10 nm thick pseudomorphic $Ge_{0.842}Sn_{0.158}$ QW embedded into two 145 nm thick Ge layers. Due to B-diffusion from the BN crucible of the effusion cell, the p-type background doping of the intrinsic Ge is

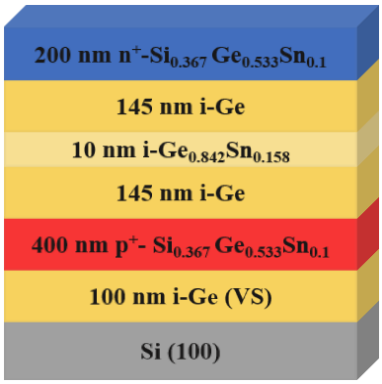

Figure 1. Schematic layerstack of the $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$-SCH-structure with nominal thicknesses and compositions.

$N_A = 1 \cdot 10^{16}\ cm^{-3}$. The p-type background doping of the $Ge_{1-y}Sn_y$ QW is in the range of $N_A = 1 \cdot 10^{17}\ cm^{-3}$ [10]. For a good ohmic contact a highly Sb doped, 200 nm thick $Si_{0.367}Ge_{0.533}Sn_{0.1}$ layer with a donor concentration of $N_D = 1 \cdot 10^{19}\ cm^{-3}$ was grown. Further details of the growth process are provided in [11].

B. Device Fabrication

The circular mesa was fabricated in a single-mesa-process. A scanning electron microscope (SEM) image of the final device is depicted in Fig. 2. The circular mesa is electrically connected with two contact pads. The top contact is implemented as ring-structure for electro-optical operation. During the fabrication process, all cleaning steps of the semiconductor surface are done consecutively with acetone, isopropanol, O_2-plasma, HF (2.5 %) and HCl (12.5 %). The mesa, the oxide windows and the metallization are patterned with optical contact lithography. Subsequent to etching processes, the removal of the photoresist took place in a O_2-plasma. The etching of the semiconductor and the metallization proceeded via inductive-coupled-plasma reactive-ion-etching in an HBr-plasma. For passivation a 300 nm thick SiO_2 layer is deposited at 250 °C via plasma-enhanced chemical-vapor-deposition using TEOS and O_2 as precursor. The contact windows were etched in a CHF_3-plasma with reactive-ion-etching and finally opened with buffered HF. The metallization consists of two layers. After cleaning of the semiconductor surface, a 50 nm Ti layer was deposited by evaporation, followed by a 1.8 µm thick sputtered Al layer. Here the Ti layer acts as a diffusion barrier to avoid Al spiking.

C. Experimental Setup

The $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$-SCH-diode was measured in a closed-cycle cryostat in combination with a four-wire DC-measurement setup (KEITHLEY 4200 SCS). The samples were electrically connected via four bond wires to a printed circuit board (PCB) which is directly placed into the sample holder of the cryostat. The pins of the PCB are connected to four coaxial wires which are feed through a vacuum tight connector out of the cryostat and connected with the source measurement unit (SMU).

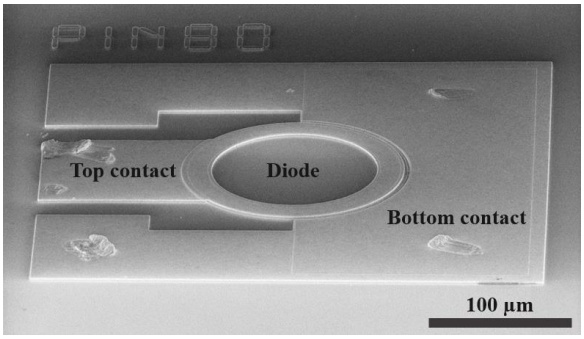

Figure 2. SEM image of the fabricated diode. The top contact, bottom contact and the diode are marked.

The current-voltage characteristics of the diode was measured in Kelvin configuration, i. e. no wire-resistance is involved. The minimum detectable current of the measurement setup is 1 pA. The He-cooling enables a temperature range from 300 K to ~8 K.

III. Results and Discussion

A. XRD Analysis

Fig. 3 shows the asymmetrical HR-XRD reciprocal space map (RSM) around the (-2-24) Bragg reflex with the individual peaks for the Si substrate, the Ge, the $Si_xGe_{1-x-y}Sn_y$ and the $Ge_{1-y}Sn_y$ QW labelled accordingly. The Ge peak contains the Ge VS and the intrinsic Ge region. Furthermore, the pseudomorphic as well as the relaxation line are shown.

As indicated by the relaxation line, the intrinsic Ge and the Ge VS layers are fully relaxed with respect to the underlaying Silicon substrate.

In contrast, the grown $Si_xGe_{1-x-y}Sn_y$ is slightly tensile strained ($\varepsilon_{\parallel} = 0.0030$). We attribute this to a slight difference in composition resulting in a strained layer and therefore in a change in the out-of-plane lattice constant $a_{\perp}$.

Most importantly, the $Ge_{1-y}Sn_y$ QW has the same in-plane lattice constant $a_{\parallel}$ as the underlaying Ge and $Si_xGe_{1-x-y}Sn_y$, thus confirming the pseudomorphic growth

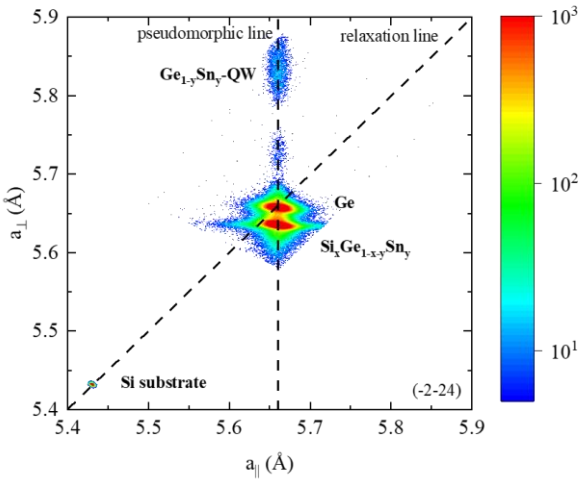

Figure 3. RSM around the (-2-24) Bragg peak of the $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$ -heterostructure.

of the active layer. To obtain the Sn concentration we calculated the relaxed lattice parameter a_0 out of the in-plane and out-of-plane lattice parameters [12]. Using Vegard's law, we can calculate the Sn concentration to be 15,8 %.

B. *Electrical Characterization*

The current-voltage characteristics of a circular mesa with a radius of 80 µm were recorded in steps of 20 K from 300 K to 20 K and an additional measurement was performed at the lowest temperature of 8 K. The voltage range was set from -1 V to 1 V with a step size of 0.01 V.

The temperature-dependent current density, normalized to the area of the mesa, is presented in a semi-logarithmic plot in Fig. 4. For room temperature the diode has a higher reverse current (negative voltage) than theoretically expected. We attribute this to point defects and non-incorporated Sn atoms. In forward direction (positive voltage) the series resistance dominates the current-voltage characteristic of the diode. With decreasing temperature, we observe a clear diode behavior. The diode shows a strong decrease of the reverse current at an applied voltage of U_D = -1 V of more than three orders of magnitude. In the forward direction the effect of temperature is not as strong as in reverse direction. However, a decrease of the current density is observed as well, i.e. the current density decreases from 34 A/cm^2 to 1.1 A/cm^2 for temperatures of 300 K and 8 K, respectively.

At temperatures above 200 K the series resistance dominates the current-voltage characteristic of the diode. Due to heating of the semiconductor and the semiconductor-metal interface there is no linear behavior between current and voltage in the series resistance regime.

For temperatures lower than 200 K a clear exponential rise of the current in the ideal diode regime can be observed. In this regime a determination of the ideality factor is possible, according to (1).

$$\eta(m,T) = q_e \cdot \log(e) / (k_B \cdot T \cdot m) \qquad (1)$$

Here q_e is the elementary charge, k_B the Boltzmann constant, T the absolute temperature and m the slope of the current density in a semilogarithmic plot.

For temperatures between 8 K and 200 K m is calculated by a linear fit in the complete ideal diode regime. Due to the lack of an ideal diode regime, temperatures above 200 K are not evaluated. With (1) the ideality factors are calculated and plotted in Fig. 5 as a function of the reciprocal temperature. We find a linear behavior of the ideality factor with the reciprocal temperature. This is due to a constant slope of the current-voltage characteristics in the ideal diode regime for all temperatures between 8 K and 200 K.

For a pn-diode, the slope of the ideal diode regime should change with respect to temperature and the ideality factor should stay constant. The change of the ideality factor of the examined diode might be attributed to other recombination mechanisms, e. g. radiative recombination in the QW or tunneling enhanced interface recombination [13] at the hetero-interfaces $Si_xGe_{1-x-y}Sn_y$/Ge and Ge/$Ge_{1-y}Sn_y$ in the intrinsic region of the diode.

The linear extrapolation of the calculated ideality factors up to room temperature allows us to extract the ideality factor at room temperature.

$$\eta(300\ \mathrm{K}) = 1.22 \pm 0.03 \qquad (2)$$

With this ideality factor, we can attribute the dominant current in the diode to be a diffusion current.

More information about the dominant mechanism of current generation in the reverse direction can be obtained from Arrhenius fits to the data. For this purpose, the current density at U_D = -1 V over the reciprocal temperature is shown in Fig. 6.

One can see that there exists a nonlinear relation between the current density at U_D = -1 V and the reciprocal temperature. This could indicate that there are multiple mechanisms involved in the current generation. For low temperatures the reverse current saturates at a level of $J_{D,-1V}$ = 10 nA/cm^2. Thus, one conduction mechanism

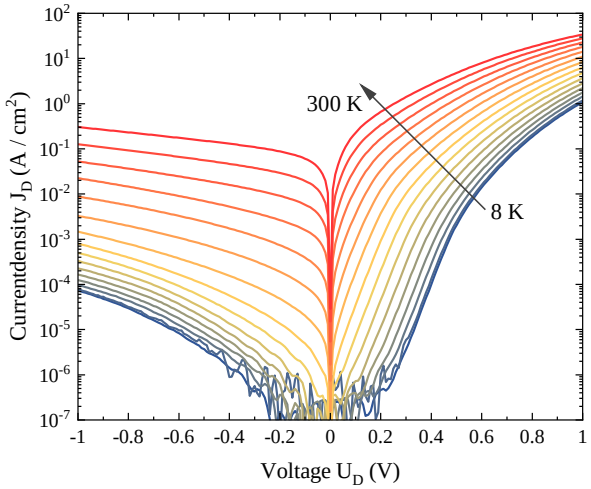

Figure 4. Temperature dependent current density-voltage characteristics from 300 K to 8 K in steps of 20 K.

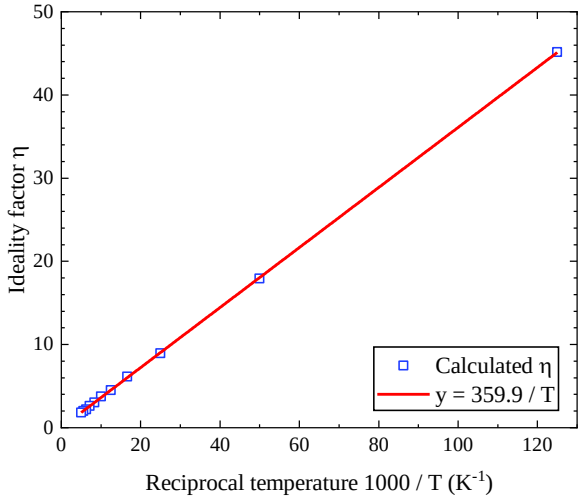

Figure 5. Calculated ideality factors and linear fit as function of the reciprocal temperature

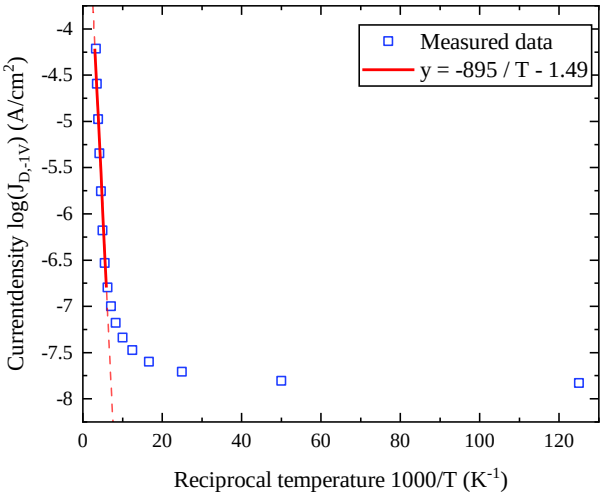

Figure 6. Current density at a voltage of -1 V as a function of the reciprocal temperature.

cannot be eliminated by reducing the temperature to 8 K. Considering the heterostructure, defects like threading dislocations could lead to such a behavior.

However, over a temperature range of 300 K to 180 K, the data can be fitted accordingly to

$$\log(I_{D,-1V}(T)) \sim -E_A \cdot \log(e) / (k_B \cdot T). \quad (3)$$

From the slope, we can determine the activation energy to

$$E_A = (178 \pm 16)\ \text{meV}. \quad (4)$$

Finally, the ideality factor of the diode is suitable for applications as a detector. The reverse current at room temperature is still too high for a good signal-to-noise ratio. This can be improved by an operation at low temperatures. To utilize the structure as emitter, a recombination dominated current with an ideality factor of 2 would be expected. This could be achieved with a thicker intrinsic $Ge_{1-y}Sn_y$ layer or a multi QW structure. With the high Sn content of 15.8 % in the pseudomorphic $Ge_{1-y}Sn_y$-QW, the direct bandgap should be in the range of 0.4 eV to 0.5 eV and therefor in a wavelength regime of ~2.5 µm. Further investigations of the optical responsivity and the electroluminescence of the diode are required to get an extended analysis. To achieve a low reverse current even at room temperature, an optimization of the crystal quality is necessary.

IV. Conclusion

In this work we investigated the temperature dependent electrical characteristic of a $Si_xGe_{1-x-y}Sn_y$/Ge/$Ge_{1-y}Sn_y$-SCH-diode. At temperatures below 200 K the structure shows a clear diode behavior. By extracting the slope of the current-voltage sweep in the diode regime we found a linear relation between the ideality factor and the reciprocal temperature. Via linear extrapolation of this relation we could calculate the ideality factor to n=1.22, stating that the dominating current inside the diode is a diffusion current. By investigating the reverse current at -1 V the activation energy of 178 meV is determined from a fit in the Arrhenius plot.

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