

Performance Analysis of 1-MHz Voltage-Controlled Ring Oscillator Designed in 180-nm CMOS Technology for Phase-Locked Loop

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Abstract—This paper presents a voltage-controlled ring oscillator designed and implemented in 180-nm CMOS technology to be used in a phase-locked loop. The performance of the circuit as a function of the temperature and supply voltage is measured. The measurements of the voltage-controlled oscillator are compared with the postlayout simulations.

Keywords—voltage-controlled oscillator, phase-locked loop

I. INTRODUCTION

The key component of every phase-locked loop (PLL) is a voltage-controlled oscillator (VCO) [1]. Application of VCOs today includes clock generation in high-speed microprocessors and carrier synthesis in communication systems [2]. Most of these applications require different oscillation frequencies at different times i.e. that the oscillators are tunable in terms of output frequency. For example, a microprocessor runs with a high-speed clock for computationally-intensive tasks but for less demanding tasks it needs a low-speed clock [1]. For VCOs, as their name implies, the controlling input signal is the voltage.

The 1-MHz voltage-controlled ring oscillator in this paper is designed and processed in 180-nm CMOS technology. The VCO is built of an odd number of delay cells that are forming a ring structure as shown in Fig. 3. Fig. 1 shows the schematic of one delay cell. The cell is powered down by $pdvco$ signal. When $pdvco$ is low, the VCO begins to oscillate. The signal $pdvco$ goes through two inverters $INV1$ and $INV2$ before it arrives to the $M6$ gate and therefore has a delay comparing with $pdvco$ signal on $M7$ gate [3]. This ensures the start of the oscillations. The inverters $INV3$ and $INV4$ are added to outputs of each delay cell so the each cell is loaded with the same parasitic capacitance. To ensure proper operation of the VCO, bulks of pMOS transistors are connected to supply voltage whereas bulks of nMOS transistors are connected to ground. Each of 21 cells is driven by the current coming from the Voltage-to-current converter (V2I), shown in Fig. 2. Namely, the output frequency of ring oscillators depends on semiconductor parameters, respectively on the supply voltage [4]. So, these oscillators require improved supply rejection. This is ensured with V2I converter, which converts control

voltage (V_{ctrl}) into the current supplying the cells. The amount of that current will depend on V_{ctrl} , considering that V2I will give the highest current for $V_{ctrl} = 0$ V and for every greater V_{ctrl} the current will be lower. So, the voltage that controls the operation of the VCO is V_{ctrl} . The VCO circuit is designed and presented in [3]. This paper gives the measurements and comparison with simulations.

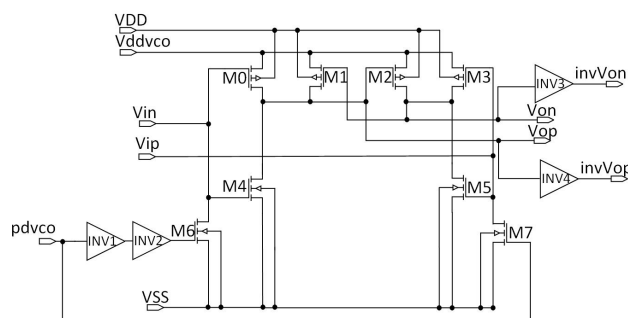


Fig. 1. Schematic of a single delay cell.

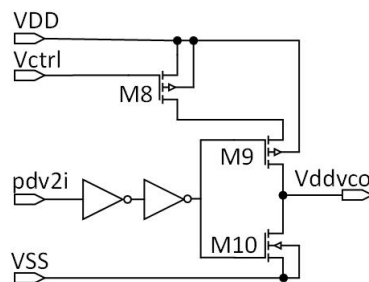


Fig. 2. Schematic of V2I converter.

This paper is organized in five sections. Section II presents an overview of the supply voltage dependence. Temperature dependence results are presented in Section III. Section IV compares measured results of the manufactured chips with simulation results. Finally, Section V brings the conclusion.

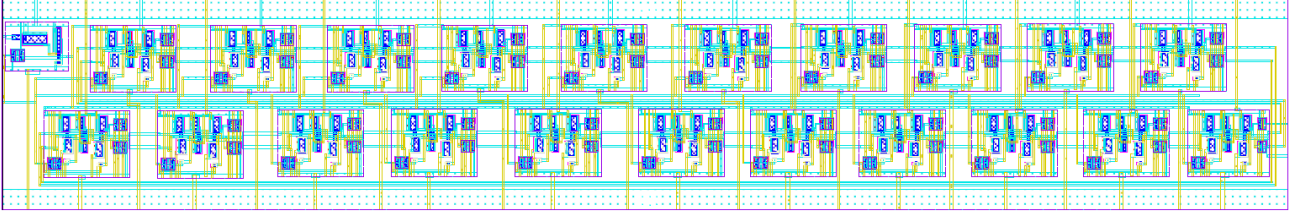


Fig. 3. Layout of the voltage-controlled ring oscillator consisting of 21 cells and V2I converter (top left).

II. SUPPLY VOLTAGE DEPENDENCE

The measurement setup is based on National instruments PXIe-1095 platform. Three PXI-4139 source measure unit (SMU) modules are used for the measurements. The first module provides the supply voltage for the VCO, the second module provides 3.3 V for the 10 pads and the third module provides the control voltage V_{ctrl} which is a variable. A fourth module is DMM (digital multimeter) and it is connected to a Pt100 sensor used to measure the temperature in the test chamber. The output frequency of the VCO is measured with the frequency counter Keysight 53220A. The measurement process is automated in LabVIEW so that V_{ctrl} is swept from 0 V to 1 V in 50 mV steps for three different supply voltage values: nominal (1.8 V), decreased by 10% (1.62 V) and increased by 10% (1.98 V). The frequency characteristics measured for 10 chip samples with the nominal supply voltage at room temperature are presented in Fig.4. Table I contains standard deviation σ and values of output frequency matching the characteristics in Fig. 4.

TABLE I
AVERAGE FREQUENCY AND σ FOR $V_{DD} = 1.8$ V AND $\bar{T} = 22.4$ °C
FOR 10 SAMPLES.

V_{ctrl} [V]	f [MHz]	σ [kHz]
0	2.69	19.3
0.1	2.62	19.0
0.2	2.53	18.7
0.3	2.43	18.4
0.4	2.29	18.1
0.5	2.12	18.0
0.6	1.87	17.9
0.7	1.58	16.7
0.8	1.28	15.1
0.9	0.99	13.3
1	0.71	10.8

The characteristics show that, for the nominal supply voltage and room temperature, the VCO achieves the design goal because it provides output frequency of approximately 1 MHz for the control voltage V_{ctrl} around 0.9 V.

An important parameter when designing a VCO for a PLL is the frequency derivation by control voltage called VCO gain or K_{VCO} . It is desirable to minimize the variation of K_{VCO} across the tuning range of the VCO for better settling behavior of a PLL [5]. Fig. 5 plots

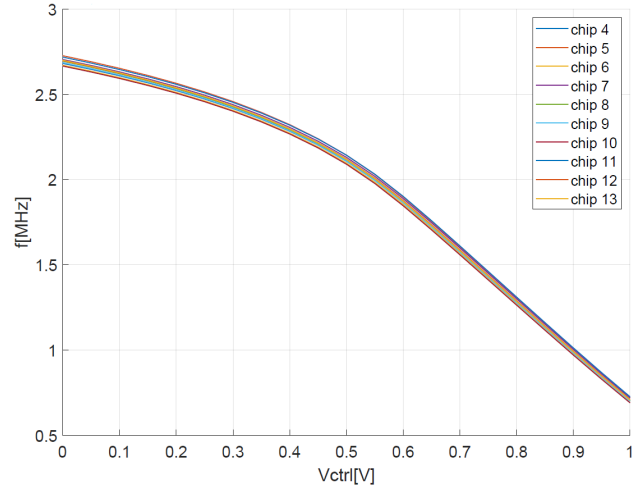


Fig. 4. Measured frequency vs. V_{ctrl} for $V_{DD} = 1.8$ V and room temperature ($\bar{T} = 22.4$ °C).

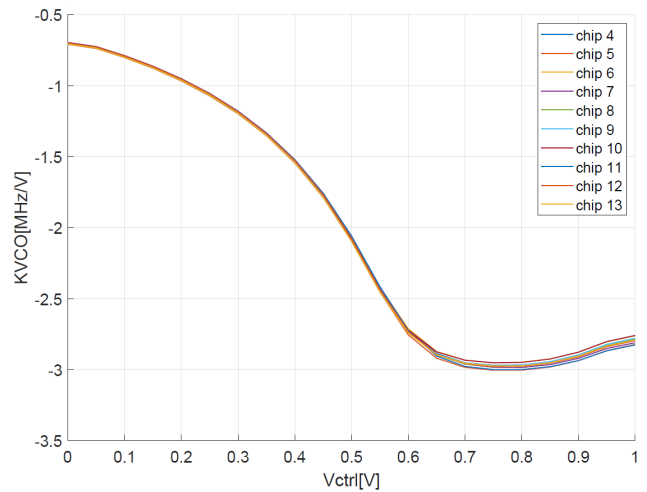


Fig. 5. Measured VCO gain vs. V_{ctrl} for $V_{DD} = 1.8$ V and room temperature ($\bar{T} = 22.4$ °C).

the K_{VCO} versus V_{ctrl} for the nominal supply voltage of 1.8 V and room temperature. The slope of the curves for all 10 chip samples indicate that the characteristics are approximately constant around the value of V_{ctrl} from 0.6 V to 1 V required for the desired frequency of 1 MHz.

Table II shows the results of the VCO output frequency and standard deviation σ for the supply voltage decreased by 10% from the nominal value to 1.62 V. The change

of supply voltage to lower values causes slightly lower output frequency of the VCO, so the targeted 1 MHz output is achieved already for $V_{ctrl} = 0.7$ V, while the standard deviation is approximately the same as for the nominal supply voltage.

TABLE II
AVERAGE FREQUENCY AND σ FOR $V_{DD} = 1.62$ V AND $\bar{T} = 22.4$ °C FOR 10 SAMPLES.

V_{ctrl} [V]	f [MHz]	σ [kHz]
0	2.34	17.8
0.1	2.26	17.4
0.2	2.17	17.3
0.3	2.05	16.8
0.4	1.89	16.7
0.5	1.66	16.6
0.6	1.38	15.7
0.7	1.08	13.9
0.8	0.79	11.9
0.9	0.52	9.5
1	0.28	6.6

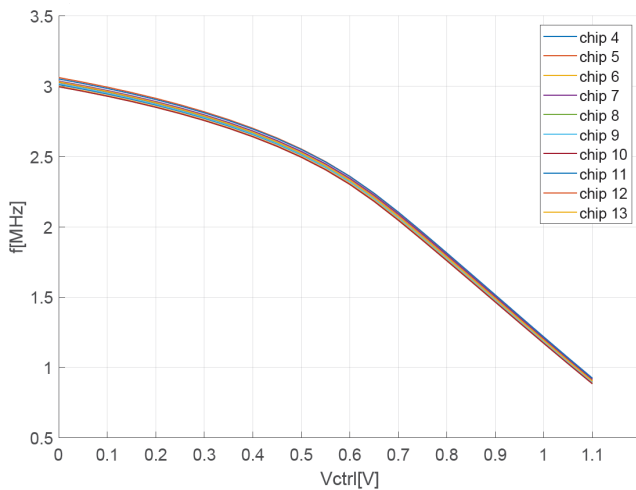


Fig. 6. Measured frequency vs. V_{ctrl} for $V_{DD} = 1.98$ V and room temperature.

Similarly, the increased supply voltage by 10% causes the VCO to give the desired output for slightly higher control voltage of 1 V with $\sigma = 14.4$ kHz. This is shown in Fig.6. The measurements for the supply voltage range of +/-10% from the nominal value show that there is a tendency of variation of the VCO output frequency with the variation of supply voltage. This is understandable due to the fact that ring oscillators typically provide decreased frequencies if the supply voltage is reduced [6].

Before the manufacturing of the chip, simulations with extracted parasitic components are conducted in Cadence Virtuoso tool. The results of these simulations for the output frequency of the VCO are different from the measurements. Table III shows the comparison of the results of simulations and measurements for the VCO,

when supply voltage is altered +/-10% and for the control voltage of 1 V.

TABLE III
COMPARISON OF SIMULATIONS AND MEASUREMENT RESULTS FOR $V_{ctrl} = 1$ V.

VDD	frequency	
	simulations	measurements
1.62 V	0.38 MHz	0.28 MHz
1.8 V	1.18 MHz	0.71 MHz
1.98 V	2.18 MHz	1.19 MHz

The output frequency of the processed and manufactured VCO is lower than the frequency in simulations. This is expected because of the parasitic resistances and capacities in the layout. This effect is also desirable because the required frequency is achieved for lower V_{ctrl} . There are two sources of possible errors: V2I and ring oscillator. The ring oscillator operates in a wide voltage range and the extraction of the capacities is probably not as good as we expected. The influence of the V2I converter is probably smaller because it regulates only the DC current flowing into the ring oscillator.

III. TEMPERATURE DEPENDENCE

The manufactured chips are supposed to be characterized in a temperature range from -40 °C to 75 °C. Due to the imperfections of the temperature chamber, reached temperatures that were closest to these were approximately -32 °C and 73 °C. Fig. 7 presents the results of measurements for this temperature range and nominal supply voltage. 10 chip samples were measured for each temperature.

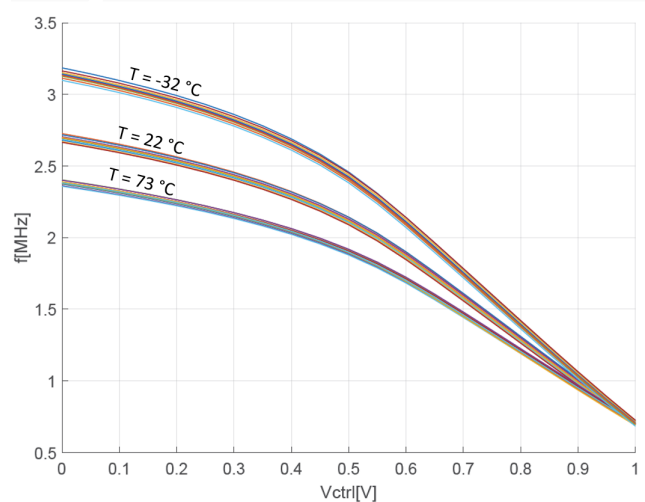


Fig. 7. Measured frequency vs. control voltage for $T = -32$ °C, 22 °C, 73 °C and $V_{DD} = 1.8$ V.

At higher temperatures, the output frequency of the VCO is lower. The divergence between the characteristic decreases as the control voltage increases. The output frequency of 1 MHz is achieved for the value of V_{ctrl} located in the area where the characteristics are only

slightly moved apart. The result is satisfying because the targeted output on temperature extremes is achieved for approximately the same V_{ctrl} as for the room temperature. K_{VCO} for the same temperature range is shown in Fig.8. At temperature extremes, K_{VCO} varies $\pm 17\%$ from the nominal value achieved on room temperature.

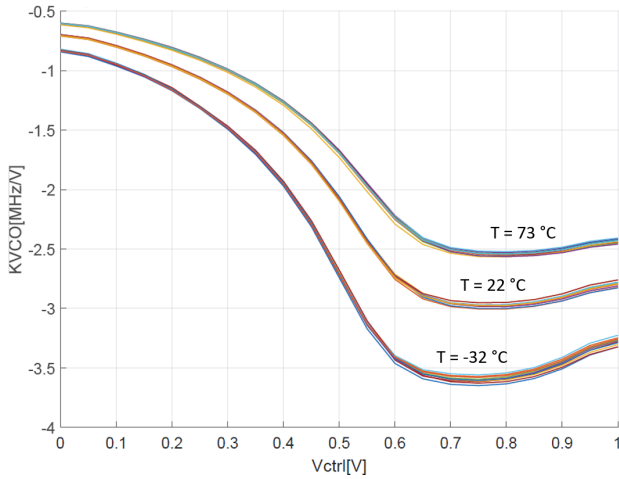


Fig. 8. Measured K_{VCO} vs. control voltage for $T = -32\text{ }^{\circ}\text{C}$, $22\text{ }^{\circ}\text{C}$, $73\text{ }^{\circ}\text{C}$ and $V_{DD} = 1.8\text{ V}$.

For the supply voltage altered $\pm 10\%$ across the temperature range of $-32\text{ }^{\circ}\text{C}$ to $73\text{ }^{\circ}\text{C}$, the output frequency characteristics show good results because V_{ctrl} necessary for targeted VCO output is similar as for the room temperature. This is shown in Fig. 9 and Fig. 10. During the measurements it is established that for the minimum supply VCO operates near it's limit of V_{ctrl} and stops functioning at lowest output frequency of 0.5 MHz. The measurement in LabVIEW is then adapted so that V_{ctrl} is swept from 0 to 0.9 V. This is visible in Fig. 9, as the characteristics for the temperature extremes are slightly shorter than nominal.

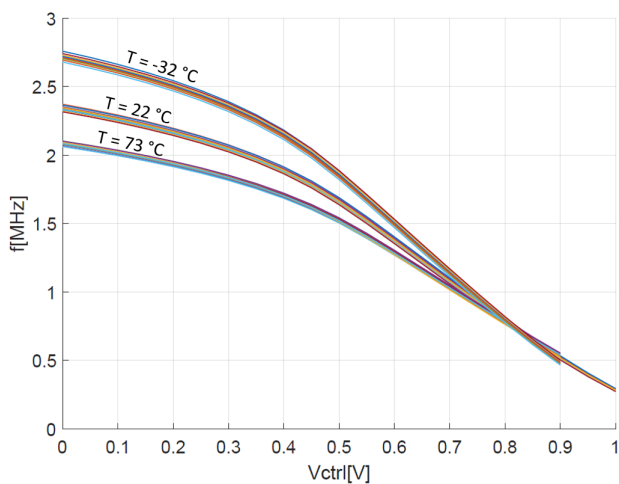


Fig. 9. Measured frequency vs. control voltage for $T = -32\text{ }^{\circ}\text{C}$, $22\text{ }^{\circ}\text{C}$, $73\text{ }^{\circ}\text{C}$ and $V_{DD} = 1.62\text{ V}$.

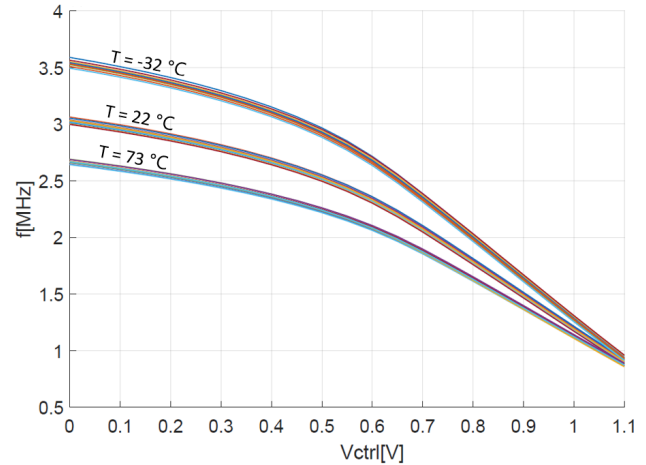


Fig. 10. Measured frequency vs. control voltage for $T = -32\text{ }^{\circ}\text{C}$, $22\text{ }^{\circ}\text{C}$, $73\text{ }^{\circ}\text{C}$ and $V_{DD} = 1.98\text{ V}$.

IV. COMPARISON OF PROCESSED CHIP AND POSTLAYOUT SIMULATIONS

Before the manufacturing the chip is simulated in Cadence Virtuoso tool. Postlayout simulations are conducted for the nominal corner ($T = 27\text{ }^{\circ}\text{C}$ and $V_{DD} = 1.8\text{ V}$) with extracted RC parasitic components included. The results of postlayout simulations showed that the VCO oscillates at lower frequencies when extracted parasitic components are taken into account. Table IV shows the comparison of the VCO output between the postlayout simulation results and measurement results of the processed and manufactured chip. Targeted output frequency of the VCO in postlayout simulations is gained for V_{ctrl} slightly above 1 V, more accurate 1.05 V. For this control voltage, the output frequency in simulations was 1.18 MHz.

TABLE IV
COMPARISON OF SIMULATIONS AND MEASUREMENT RESULTS, $V_{DD} = 1.8\text{ V}$, $T = 22\text{ }^{\circ}\text{C}$.

Vctrl	frequency	
	postlayout	manufactured
0 V	5.44 MHz	2.68 MHz
100 mV	5.31 MHz	2.62 MHz
200 mV	5.14 MHz	2.53 MHz
300 mV	4.93 MHz	2.43 MHz
400 mV	4.68 MHz	2.29 MHz
500 mV	4.34 MHz	2.12 MHz
600 mV	3.88 MHz	1.87 MHz
700 mV	3.29 MHz	1.58 MHz
800 mV	2.67 MHz	1.28 MHz
900 mV	2.06 MHz	0.991 MHz
1 V	1.46 MHz	0.707 MHz
1.05 V	1.18 MHz	0.574 MHz

However, when manufactured chip was measured, smaller V_{ctrl} was required to gain the targeted frequency of 1 MHz. Precisely, the output frequency of 0.99 MHz is obtained for the control voltage of 0.9 V. So for the same

control voltages, the measured output frequencies of the VCO are smaller than those gained with simulations, as it is shown in Table IV. The reason of this difference lies in the fact that processed and manufactured chip has some parasitic resistances and capacities that are not included in Cadence Virtuoso postlayout simulations, even though these simulations give results with RC parasitic components of the layout included.

V. CONCLUSION

The performance of the 1-MHz voltage-controlled ring oscillator manufactured in 180-nm CMOS technology is evaluated. The measurement results of the manufactured VCO show that there is a small output frequency variation with the change of work conditions, temperature and supply voltage. The supply voltage decreased by 10% results in a smaller output frequency which means that a smaller control voltage is required for the desired output frequency. Similarly, increased supply voltage results in a higher output frequency and V_{ctrl} . Regarding the temperature dependence, chip samples are tested in a temperature range from $-32\text{ }^{\circ}\text{C}$ to $73\text{ }^{\circ}\text{C}$ for the nominal supply voltage and $\pm 10\%$. The results show that the targeted output frequency of 1 MHz is achieved for approximately the same V_{ctrl} value as for room temperature, for all three different supply voltages. The measurement results of the manufactured VCO are compared with postlayout simulation results. The comparison shows that on manufactured

chip, the required frequency is achieved for smaller V_{ctrl} than in simulations. The difference is caused by parasitic resistances and capacities in the layout.

ACKNOWLEDGEMENT

This work is supported by the Croatian Science Foundation (HRZZ) within the project Fast switching converters based on GaN devices and resonant architectures FASCON (IP-2019-04-8959).

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