Abstract—The paper is focused on the design and analysis of a Voltage-to-Frequency Converter (VFC) that was implemented in 130 nm CMOS technology. The proposed VFC was designed using the bulk-driven technique and can reliably work with the power supply voltage of 0.4 V. Since its basic building block is a Fully Differential Difference Amplifier (FDDA), the proposed VFC has a differential output. Therefore, the high output frequency dynamic range ($\Delta f_{OUT}$ 3.45 kHz for the input range of 0-10 mV) as well as high sensitivity (348.8 Hz/mV) were obtained. The presented VFC can be used in complex ultra-low-voltage systems, where it would provide on-chip current consumption measurement.

I. INTRODUCTION

Towards increasing battery life of today’s portable devices, the development of integrated circuits (ICs) is mainly based on the the ultra-low-voltage (ULV) and low-power (LP) design techniques and approaches. Nanoscale CMOS technologies bring opportunity to design ICs with ultra-low value of the supply voltage, and in this way, also the current consumption of digital ICs can be decreased. On the other hand, the power consumption of analog ICs usually depends on required signal-to-noise (SNR), and therefore, it does not decrease by scaling down the supply voltage. Moreover, the ultra-low value of the supply voltage also reduces the dynamic range (DR) of analog ICs. To overcome these drawbacks of ULV ICs, new design techniques, e.g. bulk-driven approach [1]–[4] and novel topologies of analog ICs have be to introduced.

One of the basic issue in complex mixed-signal Systems-on-Chip (SoC) is to ensure the synergy between the analog and digital supply voltage domains, especially in the case of the interface between the analog and digital parts. In the conventional mixed-signal ICs, the analog signal is usually digitized at the hand of analog-to-digital converter (ADC). However, in some cases, this is not the appropriate solution from the power consumption point of view. The simpler and low-cost approach is to convert the analog signal using the quasi-digital converter such as VFC [5]–[9]. Generally, the VFC is a voltage-controlled oscillator, which frequency is linearly proportional to the control (input) voltage. The output signal is equivalent to a serial digital signal that can be directly connected to the microprocessor for further processing. With the proper design, it is possible to obtain the performance of a conventional ADC. Since the VFC has a single (serial) output, disadvantage could be a relatively long conversion time. However, due to its quite simple topology, it can be a better solution for analog-to-digital conversion in many control and measurement electronic systems integrated on the chip than the ADC approach [9].

In this paper, the design of a ULV VFC based on the differential topology is presented, and its main parameters are analyzed. In Section II, the proposed VFC is described. Achieved results obtained by simulation are presented in Section III. In the last section, the achieved results are discussed.

II. PROPOSED VOLTAGE-TO-FREQUENCY CONVERTER

The general block diagram of the proposed VFC is shown in Fig. 1. The designed VFC is based on the charge-balance approach. Firstly, the input voltage is converted into current and then, transformed into pulses using the current integrator and control circuit. The VFC has a differential input and output and therefore, its main advantage is the high dynamic range and sensitivity with respect to the conventional single-ended topology.

![Fig. 1. General block diagram of the proposed VFC](image-url)

Detail schematic diagram of the proposed ULV VFC circuit is depicted in Fig. 2. The circuit was designed in 130 nm CMOS technology and can reliably operate at the supply voltage of 0.4 V. As can be observed in Fig. 2, the proposed VFC consists of three main parts: gain stage, voltage-to-current (V-I) conversion stage and current-to-frequency (I-F) conversion stage. Considering the differential topology, devices in the both branches of the proposed VFC are the same. Passive devices (resistors and capacitors) have the same values while the transistors have the same size (channel width and length).

The first (gain) stage was used to set the appropriate voltage gain, on which the VFC’s sensitivity depends. The slope of the VFC transfer characteristic can be changed by varying the gain. The gain stage is formed by a pseudo FDDA (PFDDA) based on the rail-to-rail bulk-driven input stage, which is
Fig. 2. Schematic diagram of the proposed VFC

presented in [10] and the feedback network consisting of resistors $R_1-R_3$. To avoid the loading effect, in our case, the values of 10 kΩ, 100 kΩ and 100 kΩ for resistors $R_1$, $R_1$ and $R_3$ were chosen, respectively. The output resistance of the PFDDA is in order of kΩ but still low enough for neglecting the loading effect. The differential gain of the first stage can be expressed as follows

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}B} = \frac{A_{OL}}{1 + A_{OL}\frac{R_1}{2R_2}},$$  \hspace{1cm} (1)

where $A_{OL}$ is an open-loop gain of the PFDDA and $R_2 = R_3$. If $A_{OL} \gg B$ the differential gain of the first stage can be given by

$$A_{CL} = \frac{1}{B} = \frac{2R_2}{R_1},$$  \hspace{1cm} (2)

Since the PFDDA presented in [10] was used, Eq.2 cannot be considered in the design phase because the relation $A_{OL} \gg B$ is not satisfied in this case. The open-loop gain is not sufficiently large to be neglected in Eq 1. Additionally, it is important to note that open-loop gain of the PFDDA ($A_{OL}$) can vary with the input common-mode voltage ($V_{COMM}$), which might provide an additional gain variation of the gain stage. For this purpose, we investigate the dependence of the open-loop gain $A_{OL}$ on the input common-mode voltage of the PFDDA (in Section III).

In order to ensure conversion of voltage to current, the V-I conversion stage was employed in the proposed VFC (Fig. 2). This block generates an output current which is proportional to the input voltage. Because of the differential structure of VFC, for the simplicity point of view, the further description will be presented for the single output. Transistor $M_1$ driven by the PFDDA and resistor $R_4$ connected to the negative feedback loop form the high linear voltage-controlled current source [9], [11]. Since the PFDDA together with transistor $M_1$ represent a voltage follower, the output current $I_1$ is directly proportional to the voltage $V_1$. If we neglect the input offset voltage of the PFDDA ($V_{offset}$), the output current $I_1$ of the V-I conversion stage can be expressed as follows

$$I_1 = \frac{V_1 + V_{offset}}{R_4} \approx \frac{V_1}{R_4}$$  \hspace{1cm} (3)

The last block of the proposed VFC is a I-F conversion stage. The output current from the V-I conversion stage is firstly integrated and then transformed into the pulses using control circuitry. Current $I_1$ is mirrored using the current mirror formed by transistors $M_3$ and $M_4$. In order to minimize the current consumption of the VFC, the current through transistor $M_4$ ($I_{char}$) is lower than $I_1$ and can be expressed as

$$I_{char} = I_1B = \frac{V_1}{R_4}B,$$  \hspace{1cm} (4)

where $B = 1/6$ is the current mirror (transistors $M_3$ and $M_4$) ratio.

The timing diagram of the VFC’s operation principle is shown in Fig. 3. In the charging phase, charging current $I_{char}$ flows into capacitor $C_1$. In this phase, transistors $M_7$ and $M_9$ are turned off. The voltage across capacitor $C_1$ is sensed...
by comparator $K_1$ with the hysteresis and compared to the reference voltage $V_{\text{REF}}$. The reference voltage was supplied externally (off-chip) and was set to 200 mV. High ($V_H$) and low ($V_L$) values of the comparator threshold voltage were set to $V_{\text{REF}} \pm 100$ mV. If the voltage drop across capacitor $C_1$ is higher than $V_H$, the comparator changes its output state from log 0 to log 1 (generates a pulse at the output) and turns transistor $M_9$ on. In this moment, capacitor $C_1$ starts to discharge through transistor $M_9$. If we consider that turn-on resistance of $M_9$ is $R_{\text{ON,M9}}$, the discharge current $I_{\text{dischar}}$ can be defined as follows

$$I_{\text{dischar}} = \frac{(V_H - V_L)}{R_{\text{ON,M9}}} = \frac{\Delta V}{R_{\text{ON,M9}}}, \quad (5)$$

At the beginning of the discharging phase, transistor $M_7$ turns off the current mirror in order to prevent the charging current from flowing. The discharging phase is finished when the voltage across the capacitor drops below the low threshold voltage $V_L$. Then the comparator changes the state and starts the charging phase.

The output frequency of the proposed VFC is indirectly proportional to sum of the charge time ($t_1$) and discharge time ($t_2$) can be expressed as follows

$$f_{\text{OUT1}} = \frac{1}{t_1 + t_2} \quad (6)$$

The charge and discharge times $t_1$, $t_2$ can be expressed according to Eq. 7 and Eq. 8

$$t_1 = \frac{\Delta V C_1}{I_{\text{char}}} = \frac{\Delta V C_1 R_4}{V_1 B} = n C_1 R_4 \quad (7)$$

$$t_2 = \frac{\Delta V C_1}{I_{\text{dischar}}} = C_1 R_{\text{ON,M9}} \quad (8)$$

where $R_{\text{ON,M9}}$ is the turn-on resistance of the discharging transistor $M_9$. The output frequency expression for the proposed VFC obtained by inserting Eq. 7 and Eq. 8 into Eq. 6 is given as

$$f_{\text{OUT1}} = \frac{1}{t_1 + t_2} = \frac{\Delta V R_4 C_1}{V_1 B} + R_{\text{ON,M9}} C_1 \quad (9)$$

and simplified as

$$f_{\text{OUT1}} = \frac{1}{C_1 (\alpha R_4 + R_{\text{ON,M9}})} \quad (10)$$

It can be observed that the output frequency depends on the time constants of charge $n C_1 R_4$ and discharge $C_1 R_{\text{ON,M9}}$ phase.

### III. Achieved Results

In this section, achieved results of the proposed VFC for the supply voltage of 0.4 V are presented. The results were obtained from Corner and Monte Carlo (MC) analyses, where the process variations as well as mismatch of devices were taken into account. The particular corners for transistors are: $TPTN$ – both PMOS and NMOS for typical process variation; $FPSN$ – fast PMOS and slow NMOS; $SPFN$ – slow PMOS and fast NMOS; $FPFN$ – fast PMOS and fast NMOS; $SPSN$ – slow PMOS and slow NMOS. The temperature range from $-20^\circ\text{C}$ to $85^\circ\text{C}$ was considered in all simulations.

As already mentioned in the previous section, the open-loop gain of the PFDDA can be influenced by the input-common voltage. Therefore, we investigate the dependence of the open-loop gain of the PFDDA on the input common-mode voltage, and the obtained results are depicted in Fig. 4. It can be observed that, in the typical case, deviation of the open-loop gain is 4.27 dB in the range of the input common-mode voltage from 0 V to 0.4 V. However, in the worst case ($FPFN$, res:max, cap:max, $T=85^\circ\text{C}$), the gain will decreases to the value of about 40 dB that can influence the gain of the VFC’s gain stage. Since the proposed VFC might be used for the high-side current consumption measurement, all results were obtained for the input-common voltage of about 0.4 V.

![Fig. 3. Timing diagram of the charging and discharging phase](image-url)

![Fig. 4. Dependence of the PFDDA gain on input common-mode voltage](image-url)
The most important feature of the VFC is its transfer characteristics which defines the dependence of the output frequency on the input voltage. In Fig. 5, the transfer characteristics for both outputs as well as for the differential output are shown. Sensitivity of the first output is 137.7 Hz/mV, while the second output has slightly higher sensitivity of 211 Hz/mV. This is mainly caused by the different common-mode voltage at the inputs and outputs of the V-I conversion block (in simulations, one input was fixed and the second one was varied), which brings behavior of the proposed differential VFC into asymmetry. If the input terminals are swapped, the transfer characteristics will be also inverted. One can observe that the differential output has higher sensitivity (348.8 Hz/mV) and the frequency range from 33 Hz to 3.4 kHz which is an advantage of the proposed differential VFC. The nonlinearity (NL) is defined by Eq. 11 as the maximum relative error between ideal (depicted as straight line in Fig. 5) and real characteristics in the investigated input voltage range from 0 V to 10 mV. NL of the first and second output is 3.13% and 8.69%, respectively. However, if the differential output $\Delta f_{OUT}$ is used, the nonlinearity about 2% in the typical case.

$$NL[\%] = \max \left\{ \frac{f_{real} - f_{ideal}}{f_{ideal}} \right\} \times 100 \quad (11)$$

In order to analyze the sensitivity of the proposed VFC, the dependence of the differential output frequency $\Delta f_{OUT}$ on the input voltage for different process corners and temperature was investigated. From Fig. 6, one can observe that, in the typical case, the sensitivity of the proposed VFC is 348.8 Hz/mV. In the best case (FPSN, res: max, cap: max, $T=+20^\circ$C), the sensitivity is 515.8 Hz/mV but the higher nonlinearity can be observed. On the other hand, the nonlinearity is low in the worst case (FPFN, res: max, cap: max, $T=-20^\circ$C), where the sensitivity drops to the value of 110 Hz/mV.

From the power consumption point of view, the proposed VFC does not achieve satisfactory results. In the worst case, the power consumption is 786 $\mu$W, while in the best case, the value of 53.7 $\mu$W can be observed. The high power consumption is mainly caused by the PFDDA, which in worst case, has power consumption of 385 $\mu$W [10]. It means that the gain stage together with the V-I conversion stage of VFC represent 97% of the total power consumption. However, considering the complexity of the PFDDA, such a value might be still acceptable. It is important to note that the presented power consumption was obtained for the worst and best process corners from the output frequency point of view. If we consider the power consumption in the best case (SNSP, res: max, cap: max, $T=-20^\circ$C), it will be only 17.71 $\mu$W, while the worst case will not change.

In this case, mismatch of $\pm 3\sigma$ as well as process variation of

---

**Fig. 5.** VFC differential output frequency vs. input voltage

**Fig. 6.** VFC output frequency vs. input voltage for different process corners

**Fig. 7.** VFC power consumption vs. input voltage for different process corners
all devices were taken into account. The mean value of $\Delta f_{OUT}$ of 1.55 kHz was obtained with the standard deviation of 1 kHz. Based on the preformed MC analysis we can conclude that a relatively high variation of the output frequency was observed, which can be caused by passive devices used in the proposed VFC.

For this purpose, we investigated and analyzed the sensitivity of the proposed VFC on the process variations using the Corner analysis. Results obtained from the Corner analysis are shown in Fig. 9, where the output frequency is normalized to the maximum output frequency in the particular transistor process corner. One can observe that the output frequency is mainly sensitive to passive device used in the designed VFC. The higher influence has been reported for capacitor $C_1$, where the deviation of the output frequency is up to 20% (with the change between the minimum and the maximum value of capacitor). In the case of resistors, the variation of about 14% in the output frequency can be observed. These variations in the output frequency correspond with the relative changes of the resistor (from -24% to 13%) and capacitor (from -17% to 13%) in the corner simulations. In order to compensate these process variations, some calibration methods or compensation techniques have to be employed [12].

The main parameters of the proposed VFC are summarized in Table I, where all process corners and the temperature range from –20°C to 85°C are considered.

### Table I
**Main parameters of the proposed VFC**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Range [mV]</td>
<td>-</td>
<td>0 – 10</td>
<td>-</td>
</tr>
<tr>
<td>Frequency Range [kHz]</td>
<td>0.003 - 1.09</td>
<td>0.033 - 3.48</td>
<td>0.056 - 5.16</td>
</tr>
<tr>
<td>Frequency Span [kHz]</td>
<td>0.109</td>
<td>3.45</td>
<td>5.106</td>
</tr>
<tr>
<td>Sensitivity [Hz/mV]</td>
<td>110.1</td>
<td>348.8</td>
<td>515.8</td>
</tr>
<tr>
<td>Nonlinearity [%]</td>
<td>-</td>
<td>-2.7</td>
<td>-</td>
</tr>
<tr>
<td>Offset Error [Hz]</td>
<td>1.3</td>
<td>33.2</td>
<td>52.2</td>
</tr>
<tr>
<td>Total Power [µW]</td>
<td>17.71</td>
<td>78.4</td>
<td>788.4</td>
</tr>
</tbody>
</table>

### Table II
**Comparison of the VGA to other works**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[13]</th>
<th>[14]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>180 nm</td>
<td>65 nm</td>
<td>130 nm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
<td>1.2 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Total Power [mW]</td>
<td>0.08</td>
<td>0.168</td>
<td>0.078</td>
</tr>
<tr>
<td>Temperature Range [°C]</td>
<td>-40 to 120</td>
<td>-30 to 80</td>
<td>-20 to 85</td>
</tr>
<tr>
<td>Input range [V]</td>
<td>0.1-1.2V</td>
<td>30 nA-60 µA</td>
<td>0-10 mV</td>
</tr>
<tr>
<td>Frequency range [Hz]</td>
<td>0.1M-1M</td>
<td>1.3k-2.49M</td>
<td>0.033-3.48M</td>
</tr>
<tr>
<td>Sensitivity [50kHz/V]</td>
<td>750kHz/V</td>
<td>41.5Hz/µA</td>
<td>348.8kHz/V</td>
</tr>
<tr>
<td>Nonlinearity [%]</td>
<td>0.009</td>
<td>±0.6</td>
<td>0.59</td>
</tr>
</tbody>
</table>

From the Table I and Table II can be observed that the proposed VFC has good linearity in a wide output frequency range that is mainly cased by the differential topology. The maximum offset error is about 52 Hz which represents only 1% of the full frequency range of VFC. The disadvantage of the proposed VFC is its relatively high power consumption mainly caused by PFDDA, which was designed as basic a building block for differential signal processing. Therefore, the power consumption can be reduced by a proper design of the gain and V-I conversion stages.

The microphotography of the designed VFC is shown in
Fig. 10. The VFC occupies chip area of 0.227 mm$^2$ with dimensions of 863 $\mu$m $\times$ 263 $\mu$m. The gain stage was placed on the left side, while the V-I conversion stage was placed in the middle of the layout. The considerable layout area is occupied by capacitors $C_1$ and $C_2$, which were placed on the right side of the layout. Proper layout techniques were employed in order to achieve good matching of the bulk-driven MOS transistors as well as all passive devices (resistors and capacitors).

IV. CONCLUSION

The differential low-voltage VFC, based on the PFDDA topology and designed in 130 nm CMOS technology, was presented. As demonstrated, the designed VFC can be used in low-voltage applications, where the supply voltage of less than 0.4 V, high dynamic range and high linearity are required. Since the proposed VFC has a rail-to-rail input voltage range, it can be used for the high-side or low-side on-chip current measurement. The future work will be focused on the design of calibration circuitry and measurement of the designed VFC.

ACKNOWLEDGMENT

This work was supported in part by the grant VEGA 1/0762/16, the Slovak Research and Development Agency under grant APVV-15-0254 and the ECSEL JU under project CONNECT (737434).

REFERENCES


