Measurement System for Characterization of a Resistor Array in 180-nm CMOS Technology

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***Abstract*—Integrated circuits are very sensitive to variations of temperature. All components used in IC design (transistors, resistors, capacitors and other components) are characterized with respect to the change of temperature by defining the temperature coefficients, usually of the first and second order. The temperature coefficient is usually specified as a fixed number for a given type of a resistor, i.e. it is assumed that the temperature coefficient does not depend on the dimension *L* (length) and *W* (width) of the resistor, which is usually not the case. This paper describes the system for characterization of the temperature coefficients of resistors having various lengths, widths and number of fingers, as well as different resistor types. The system is based on an array of resistors consisting of 20 rows and 10 columns, which is sufficient to characterize 200 resistors. Each resistor cell can be selected separately, i.e. only one cell is active during the measurement. The measurement is based on the 4-wire method, i.e. on forcing the current and measuring the voltage on the resistor. Digital circuits and analogue switches are built into the integrated circuit to enable the selection of each resistor cell.**

***Keywords*—resistor array, temperature coefficient, 4-wire sensing, Kelvin sensing**

I. INTRODUCTION

Nowadays, precise and temperature compensated operation is required in many applications. Examples are different types of oscillators, current/voltage references and others [1]–[4]. One of the critical components required for realising these systems are various types of resistors. To achieve required system performance, detailed temperature characterization of the used resistors is necessary.

Thewes et al. [5] presented a model which shows a relation between polysilicon resistors mismatch and their grain size in 0.65-µm CMOS technology. Their design consists of a resistor array arranged in rows and columns where each resistor can be selected for 4-wire measurement. A similar test structure is used in this paper. Different structures which use resistor arrays with each resistor connected directly to the pads without a switching matrix are described in [6] and [7]. Temperature characterization of polysilicon resistors to determine coefficients of CMC-R2 compact model is shown in [8].

The main goal of this paper is to describe a system which can be used to characterize resistor temperature coefficient dependence on width and length of polysilicon and diffusion resistors. These resistors are arranged in an array which consists of 20 rows and 10 columns where each cell can be selected for the 4-wire measurement. The influence of possible sources of errors on the resistor temperature coefficient characterization is taken into consideration.

This paper is organized as follows. Section II describes the architecture of a resistor array. Simulations of resistance measurements and their results are shown and discussed in Section III. Finally, a conclusion is given in Section IV.

II. RESISTOR ARRAY ARCHITECTURE

There are multiple different resistor types available in the used 180-nm CMOS technology (poly, diffusion and well resistors) which differ in their sheet resistance and temperature coefficients (T_{Ci}). The T_{Ci} of these resistors depend on their width (*W*) and length (*L*) [9] which is not listed in the device specifications where they are given as constants. The temperature dependence of a resistance can then be modelled as:

$$R(T) = R_0 \cdot (1 + T_{C1} \cdot \Delta T + T_{C2} \cdot \Delta T^2), \qquad (1)$$

where R_0 is the resistance at the nominal temperature T_0, T_{C1} and T_{C2} are the first and second-order temperature coefficients and ΔT is the difference between current temperature T and T_0.

Based on the specified first-order T_C in this technology, two resistor types are chosen for the characterization of the T_C dependence on *W* and *L*: *p+* diffusion resistor RDIFFP and *p+* poly resistor RPOLY1PC as they have the lowest positive and the highest negative T_C, respectively. Their first-order temperature coefficients are shown in Table I.

The system for T_C characterization is designed as an array of resistor cells where each cell is defined by the following parameters: number of serially connected unit resistors it is comprised of and dimensions of a single unit resistor (*W* and *L*). These parameters also define a naming convention for cells used in this paper: RP_FX_WY_LZ for RPOLY1PC and RD_FX_WY_LZ for RDIFFP, where *X* is the number of identical units (fingers), *Y* is the width *W* and *Z* is the length *L*. The resistor cells are made with

TABLE I: First-order T_C of selected resistors

Resistor type	T_{C1} [ppm/°C]
RPOLY1PC	-238
RDIFFP	1383

1, 5 or 9 unit resistors where each one of them can have four different values of widths (0.5 µm, 1 µm, 2 µm, 4 µm) and lengths (5 µm, 20 µm, 50 µm, 100 µm). Table II shows the maximum and minimum resistances for each resistor type using previously mentioned combinations.

Fig. 1 shows an example of a layout of two resistor cells. Each cell has a guard ring which is used to ensure a stable potential of a local substrate. The guard rings are connected to the external high-level voltage V_{NWELL} for diffusion resistors and to the reference voltage V_{SS} for poly resistors. Each resistor cell contains two dummy unit resistors connected to the guard ring and positioned above and below other unit resistors to achieve better matching [10]. Two columns of contacts at both ends of each unit resistor are used to reduce the resistance of a connection to the metal layer.

The measurement of each cell is performed using the 4-wire method as high accuracy is desired. Fig. 2 shows the implementation of this method where both current-forcing and voltage-sensing connections can be disconnected from the resistor cell using controllable analogue switches. Each switch is implemented as shown in Fig. 3. The dimensions of pMOS MP1 are W = 4 µm, L = 0.5 µm and of nMOS MN1 are W = 2 µm, L = 0.5 µm.

The resistor cells are organized as an array with selectable rows and columns. Only a single resistor cell can be measured at a time by selecting its corresponding row and column, i.e. when its inputs $RSEL$ and $CSEL$ are high level. Additionally, two high-level inputs FSW and SSW have to be provided to separately enable current-forcing and voltage-sensing connections.

The measured resistance is then by the definition:

$$R_M = \frac{V_V}{I_B}, \tag{2}$$

where V_V is the voltage measured by the voltmeter and I_B is the current forced by the current source. The finite input resistance R_V of the voltmeter and non-zero resistance of switches in the voltage-sensing loop introduce an error in the measurement of an actual resistance of a resistor cell. This effect can be seen when (2) is rewritten as:

$$R_M = \frac{R_{real} \cdot R_V}{R_{real} + R_V + 2R_S}, \tag{3}$$

where R_{real} is the actual resistance of a resistor cell, R_V is the input resistance of the voltmeter and R_S is the resistance of each analogue switch in on-state. It is visible that the error can be reduced by increasing input resistance of the voltmeter or reducing on-state resistance of switches. Also, a lower error is obtained when measuring lower resistance values. Usually, the on-state resistance of the switches can be neglected if R_{real} is known to be of the relatively higher value. In that case, the actual resistance of the resistor cell can be simply calculated as:

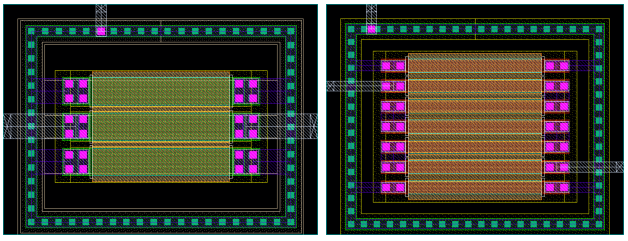
$$R_{real} = \frac{R_V \cdot R_M}{R_V - R_M}. \tag{4}$$

The encircled part of the schematic in Fig. 2 represents a basic building block of the resistor array and its layout is shown in Fig. 4. The switches and the resistor cell beneath them are placed in the right part of the block while the bus which connects them to the other blocks is placed in the left part.

The resistor array with 10 columns and 20 rows, totalling in 200 blocks is then built by placing these blocks

TABLE II: Minimum and maximum resistance in the array

Resistor type	Minimum	Maximum
RPOLY1PC	441.80 Ω	619.2 kΩ
RDIFFP	187.10 Ω	219.6 kΩ



(a) RD_F1_W1_L5 (b) RP_F5_W0.5_L5

Fig. 1: Example of a layout for both resistor types: (a) diffusion resistor with one unit and dummy units above and below the resistor, (b) poly resistor with 5 units and two dummy units.

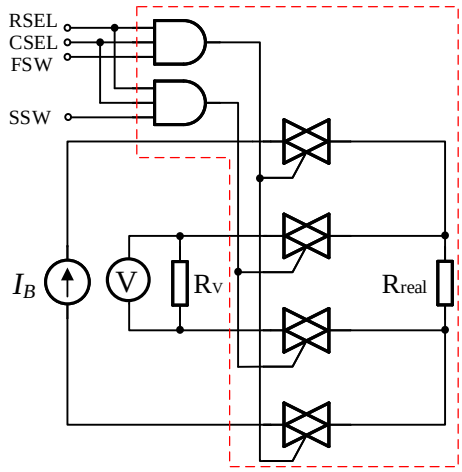
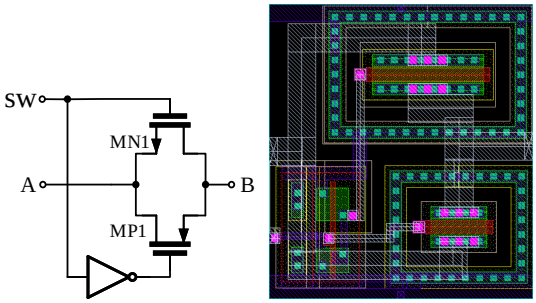


Fig. 2: Schematic of the 4-wire method for measuring resistance. R_{real} represents a measured resistor.



(a) (b)

Fig. 3: Schematic and layout of an analogue switch.

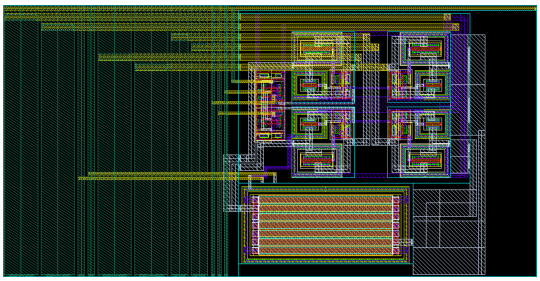


Fig. 4: Layout of a block with switches and resistor.

next to each other as shown in Fig. 5. There are 64 different blocks used, most of them being repeated 3 or 4 times to fill out the array. As previously explained, each block can be selected for measurement by setting corresponding $CSEL$ and $RSEL$ signals to high-level. Then, after also enabling switches in current-forcing and voltage-sensing loops with FSW and SSW signals, the test current flowing through FP and FN can be set and the voltage across VSP and VSN can be measured. According to the measured voltage and known test current, resistance of the selected block can be determined.

The signals for selecting particular row $RSEL_1$ to $RSEL_{20}$ and column $CSEL_1$ to $CSEL_{10}$ are generated with two separate decoders. The row and column decoders are formed using a 2-to-4 decoder with output enabling signal CS which is shown in Fig. 6(a). The column decoder shown in Fig. 6(b) is built by combining five 2-to-4 decoders which results in 16 outputs, out of which only 10 are used. Then, by combining two column decoders and an additional digital logic at the inputs, a row decoder is formed as shown in Fig. 6(c). Again, only 20 outputs of available 32 are used. The required four inputs of the column decoder and five inputs of the row decoder are externally provided through pins of the chip, the same as the shared input CS which enables outputs of decoders. Fig. 7 shows the layout of decoders on the left side and the first nine blocks on the right side. Table III lists external pins of the chip.

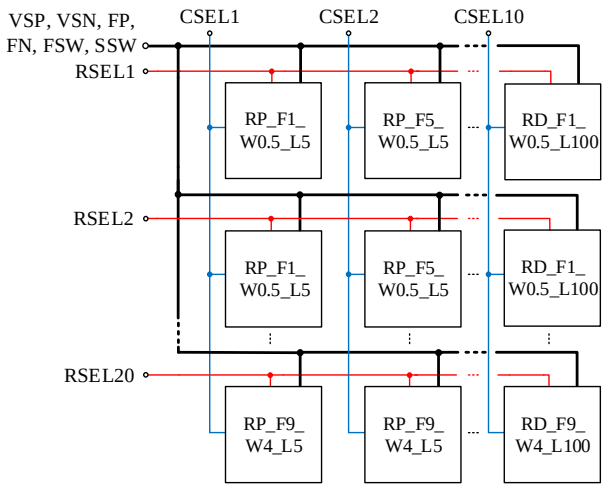


Fig. 5: Schematic of the resistor array.

TABLE III: Pins

Pin name	Description
V_{DD}	power supply
V_{SS}	reference voltage (gnd)
V_{NWELL}	n-well polarization voltage
FP	force pin (current in)
FN	force pin (current out)
VSP	voltage sense plus
VSN	voltage sense minus
SSW	sense switch select
FSW	force switch select
CS	chip select
IN_C1 to IN_C4	column select 1 to 4
IN_R1 to IN_R5	row select 1 to 5

III. SIMULATIONS AND RESULTS

As previously explained, only a single block can be measured at a time. To measure the resistance of all 200 blocks, the input signals for decoders are generated so that each 10-ms a block in the following column is measured, row by row. The simulation of this measurement for the blocks in the first row is shown in Fig. 8. This simulation is performed at the nominal conditions (T = 27 °C, V_{DD} = 1.8 V) and with parasitic components extracted from the layout of the whole design. The input resistance of the voltmeter R_V is set to 1 MΩ and the test current to 1 µA. The same approach is used in all other simulations.

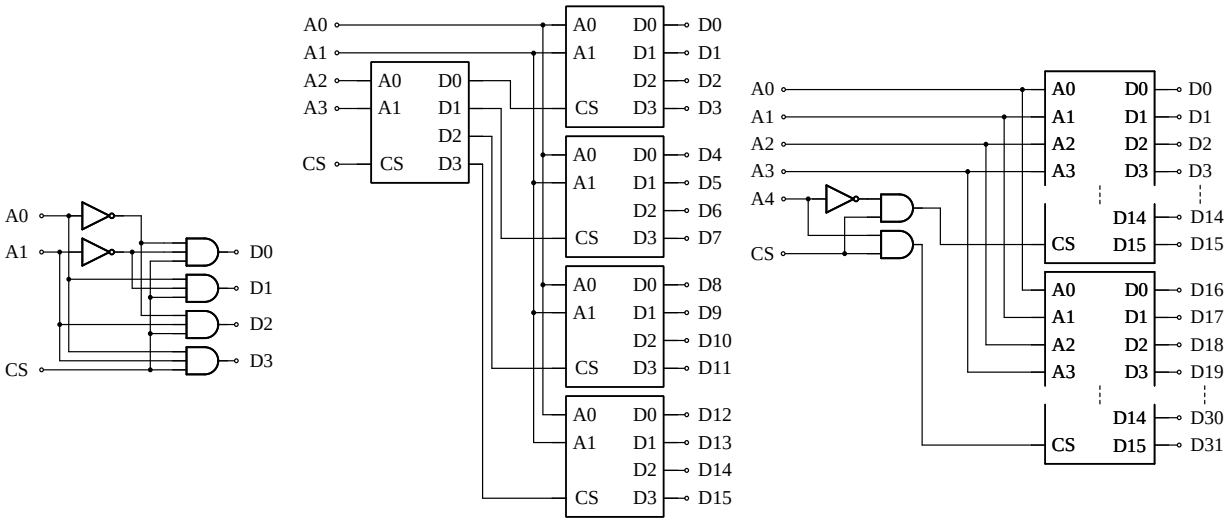
The change in temperature and the power supply voltage V_{DD} affects the value of the measured resistance. The simulations at temperatures -40 °C and 125 °C at the nominal V_{DD} are performed to compare these results with those acquired at nominal conditions. Similarly, the impact of the supply voltage variation on the measured resistance is evaluated for $\pm 10\%$ change of the nominal V_{DD} at the nominal temperature. Only a subset of the available blocks is used for simulations to show general trends and these results are presented in Table IV. As the absolute change of resistance depends on the nominal resistance, a relative change of the measured resistance is used for comparison:

$$\Delta R_r(T, V_{DD}) = \frac{R_M(T, V_{DD}) - R_M(T_0, V_{DD0})}{R_M(T_0, V_{DD0})}, \quad (5)$$

where V_{DD0} is the nominal supply voltage.

The measured resistance changes with respect to the temperature due to the temperature coefficient of resistors, as previously shown in (1). The measured resistance value of RPOLY1PC resistors decreases as the temperature rises due to their negative T_C. The opposite is true for RDIFFP resistors, for which the measured resistance increases as the temperature rises because of their positive T_C. The relative change of the measured resistance is larger for diffusion resistors as they have a larger absolute T_C value than poly resistors.

Simulations of the supply voltage variations show that the measured resistance increases for both types of resistors as the voltage increases. The cause of this error is the change of the on-state resistance of analogue switches



(a) 2-to-4 decoder (b) column decoder (c) row decoder

Fig. 6: Schematics of decoders.

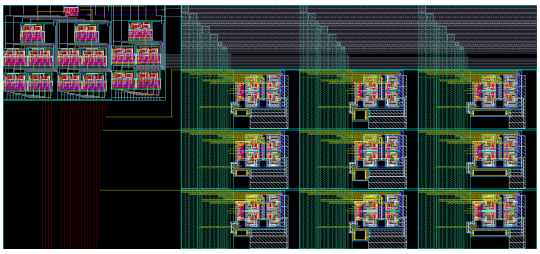


Fig. 7: Layout of a resistor array (decoders and first nine blocks).

which impacts the measured resistance. When the supply voltage is lower, the overdrive voltage $|V_{GS}-V_{TH}|$ is also lower which increases the channel resistance of transistors. This increase of the on-state resistance of switches reduces the measured resistance of the block as can be seen from (3). Similarly, the supply voltage increase reduces the on-state resistance of the switches which results in higher measured resistance.

Monte Carlo simulations with 50 samples at the nominal conditions are performed for three different blocks of both resistor types as shown in Table V. For both types of resistors the same triplets are chosen with dimensions (W and L) and a number of unit resistors such that they cover a wide range of resistances. These simulations are also performed for the same resistors as in the chosen blocks but without the measurement system. This would show the impact of the measurement system on the measured resistance. For easier comparison, the input resistance of the voltmeter is removed from the measured resistance as in (4) to obtain the actual resistance of the block. This value is then compared to the resistance measured without the impact of the measurement system. The results show that the standard deviation increases for higher resistance of a block, which is expected but is not a good indicator of the measured resistance dispersion. A better indicator is the coefficient of variation which shows dispersion relative to the value of the measured resistance. It shows that for the both cases (with and without the impact of the measurement system), a relative dispersion is higher for blocks which use unit resistors that have one small dimension. This occurs because the same deviation of one dimension results in its relative change to be higher if that dimension is small and this consequently results in higher relative resistance change. Impact of the measurement system can be seen in the mean values of the measured resistances. Measurement system decreases the measured resistance due to the nonzero on-state resistance of the switches as previously described. Resistors show similar dispersions for both cases.

Existence of leakage currents that flow through unselected blocks can change the value of the measured resistance. The main contributors to the leakage are the currents that flow from the substrate to the sources/drains of transistors inside the switches and similarly from the substrate connections to the terminals of diffusion resistors. The leakage currents obtained by the simulations are shown in Table VI. These simulations are performed by using two voltage sources where one of them with voltage values of 0.2 V or 1.1 V is connected to the external pin FP while the other one with voltage values of 0 V or 0.9 V is connected to FN. In this way, a constant 200 mV voltage drop across the resistor is achieved with

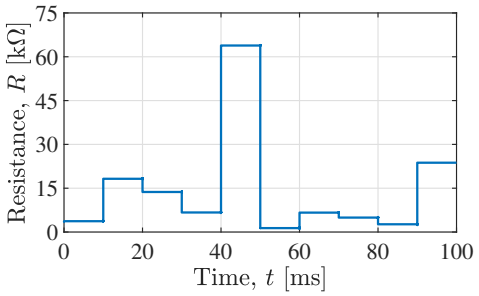


Fig. 8: Simulation of the first row measurement.

TABLE IV: Various temperature and voltage simulation results

Resistor	V_{DD} = 1.8 V T = 27 °C	V_{DD} = 1.8 V T = -40 °C		V_{DD} = 1.8 V T = 125 °C		V_{DD} = 1.62 V T = 27 °C		V_{DD} = 1.98 V T = 27 °C	
	Res (Ω)	Res (Ω)	ΔR_r (%)	Res (Ω)	ΔR_r (%)	Res (Ω)	ΔR_r (%)	Res (Ω)	ΔR_r (%)
RP_F1_W1_L5	1803.40	1848.70	2.51	1767.10	-2.01	1799.12	-0.24	1806.30	0.16
RP_F5_W0.5_L20	64.96 k	65.99 k	1.60	64.38 k	-0.90	64.79 k	-0.26	65.07 k	0.17
RP_F9_W0.5_L100	380.70 k	384.25 k	0.93	378.15 k	-0.67	380.31 k	-0.10	380.93 k	0.06
RD_F1_W1_L5	715.20	664.43	-7.10	802.90	12.26	713.29	-0.27	716.55	0.19
RD_F5_W0.5_L20	24.21 k	22.24 k	-8.13	27.53 k	13.70	24.16 k	-0.22	24.26 k	0.20
RD_F9_W0.5_L100	179.53 k	166.45 k	-7.29	200.25 k	11.54	179.18 k	-0.20	179.74 k	0.12

TABLE V: Monte Carlo simulation results (T = 27 °C, V_{DD} = 1.8 V)

Resistor	With the measurement system			Without the measurement system		
	Mean, μ (Ω)	Std dev, σ (Ω)	Coefficient of variation, σ/μ (%)	Mean, μ (Ω)	Std dev, σ (Ω)	Coefficient of variation, σ/μ (%)
RP_F1_W0.5_L5	3.74 k	270.60	7.24	3.77 k	269.40	7.16
RP_F5_W2_L20	16.65 k	604.10	3.63	16.75 k	601.50	3.59
RP_F9_W0.5_L100	617.40 k	45.65 k	7.39	621.50 k	46.03 k	7.41
RD_F1_W0.5_L5	1.35 k	104.50	7.72	1.36 k	104.60	7.69
RD_F5_W2_L20	6.91 k	257.16	3.72	6.95 k	255.40	3.67
RD_F9_W0.5_L100	220.10 k	15.32 k	6.96	221.30 k	15.51 k	7.01

TABLE VI: Leakage currents simulation results (V_{DD} = 1.8 V)

Temperature (°C)	27	27	125	125	27	27	125	125
Corner	nominal	nominal	nominal	nominal	wp	wp	wp	wp
V_{FP} (V)	0.2	1.1	0.2	1.1	0.2	1.1	0.2	1.1
V_{FN} (V)	0	0.9	0	0.9	0	0.9	0	0.9
I_{FP} (A)	-667.97 p	33.46 p	25.38 n	-623.31 p	-509.16 p	33.028 p	84.01 n	-1.09 n
I_{FN} (A)	-1.84 n	-135.08 p	-45.23 n	-841.21 p	-3.78 n	-135.68 p	-105.47 n	-1.33 n

the possibility of setting two different common-mode voltages of the resistor terminals. Then, while none of the blocks is selected, the current through each pin is measured with the currents being positive if they flow from the outside into the chip. Simulations are performed for all 8 possible combinations of temperature (27 °C, 125 °C), process corner (nominal, worst power *wp*) and input voltages (0 V and 0.2 V, 0.9 V and 1.1 V) while the supply voltage is set to the nominal value. The worst power corner and temperature of 125 °C are chosen in addition to the nominal values as the leakage currents increase in these conditions. The results show that in addition to the worst power corner and temperature increase, input voltages set to 0 V and 0.2 V also result in higher leakage currents, with the worst case being for all these conditions combined. In that case, the leakage currents reach 10% of the previously used test current of 1 µA. Therefore, the input voltages should be set to approximately half of the supply voltage for the actual measurement to reduce the error.

IV. Conclusion

This paper shows the architecture of a resistor array with 200 blocks arranged in 20 rows and 10 columns which is used for characterization of temperature coefficients of two resistor types. The resistance is measured using the 4-wire method and error sources in these measurements are explained. Temperature simulations show the dependence of the measured resistance on the temperature coefficient, while the voltage simulations show the impact of the analogue switch on-state resistance. Monte Carlo simulations demonstrate that the relative resistance dispersion changes with the respect to the unit resistor dimensions. Leakage currents can be minimised by properly setting the input voltages as shown in simulations.

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