Low-Power CMOS Frequency Comparator

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***Abstract*—This paper is focused on the design and analysis of a fully on-chip frequency comparator (FC) implemented in 65 nm CMOS technology. The proposed FC employs a digital pre-processing stage followed by a rail-to-rail input and output (RRIO) voltage comparator, with low power consumption in units of μW. Evaluation accuracy is maintained for input frequencies up to 1 MHz. The FC is designed for the supply voltage of 1.2 V. The FC accepts signals with independent duty cycles and delays, without any correlation between the signals, making it an universal building block of more complex integrated systems. Presented simulation results show robustness of the proposed topology over process, temperature and supply voltage variations (PVT). The presented FC was used in complex ultra-low power System on-Chip (SoC).**

I. Introduction and Background

Today's electronic systems implemented on a single SoC require advanced control mechanisms (changing modes, adaptive switching, etc.) in order to achieve the required performance from the functional point of view, while also improving the energy efficiency of the whole system. By utilizing this approach, effective control of complex mixed-signal integrated circuits (ICs) can be leveraged to achieve better power efficiency of the system as a whole, ultimately leading to prolonged battery life in applications such as Internet-of-Things (IoT). To implement such an adaptive control approach sensing of selected parameters, which can affect the efficiency of whole system, is required. Using the sensed parameter as an input, a control mechanism can be introduced into the system. This controller can then be used to adjust some system parameters, so that energy consumption is minimized while maintaining the performance at a level required for the function of the device.

In many applications the frequency of a signal is used to determine the appropriate operating mode of a system. To reduce the time required for the change of the operating mode, thus minimizing any unwanted effects associated with the mode switch, a reliable method of detecting the signal frequency is required. The above mentioned FC is a simple way to accomplish this task. The FC compares an input signal frequency to a reference, and evaluates if it is higher or lower than the reference signal frequency. Various implementations of the FC are possible. These can be based on purely digital or mixed-signal circuits. One digital-only implementation, described in [1], uses an edge detector, a re-triggerable monostable multivibrator and a D-type Flip-flop (DFF). Here, the multivibrator timing interval is set to a duration derived from the reference frequency. This results in the multivibrator being re-triggered before timing out if the input frequency is higher than the reference. Another approach, described in [2], is based on two separate counters, one for the input and reference signal each. Similar methods are presented in [3], [4]. Here the two signals are also driving two counters [3], or simple DFFs. The output of these is instead of direct evaluation connected to a low-pass filter (LPF). An analog comparator is then used to compare the LPFs output signals.

To the extend of authors knowledge, the number of research papers dedicated to this topic is rather limited. This presents an opportunity to introduce novel topologies suited for on-chip implementation and focusing on low power consumption, while maintaining compatibility with standard CMOS technology nodes. For these reasons, the paper presents design and analysis of a fully on-chip FC, implemented in 65 nm CMOS technology. The paper is structured as follows: Section II describes design of the FC as well as its major circuit blocks. Section III presents achieved results of the FC circuit simulation. Conclusions are drawn in Section IV.

II. Proposed FC Topology

A. Frequency comparator

A simplified schematic diagram of the proposed FC is shown in Fig. 1. It is mainly based on the topology presented in [4], with small modifications made necessary by the requirements of fully on-chip implementation. Input frequencies (F_1 and F_2) are fed to the DFFs trough edge detectors (EDs). The EDs are used because of the master-slave architecture of DFFs in the particular technology node used. The outputs of the DFFs are compared in a NAND gate, which generates a reset signal for the DFFs. In the case when $F_1 < F_2$ the output of the first DFF (Q_F1) will exhibit a smaller pulse density than Q_F2. Since the DFF output is integrated by a LPF, the mean value of signal $CTRL\_F1$ will be smaller then mean value of signal $CTRL\_F2$. If we increase the frequency of $F1$, the voltage in the node $CTRL\_F1$ will also be increase. When the frequency of F_1 is increased above F_2, the comparator will change the state of its output and indicate that $F_1 > F_2$. The designed comparator can evaluate the state of the inputs correctly even if the input and reference frequencies are significantly lower than cut-off frequency of the LPF. Details of how this is achieved are given in the following section. To ensure the reliability of the proposed FC, the initialization circuit block containing

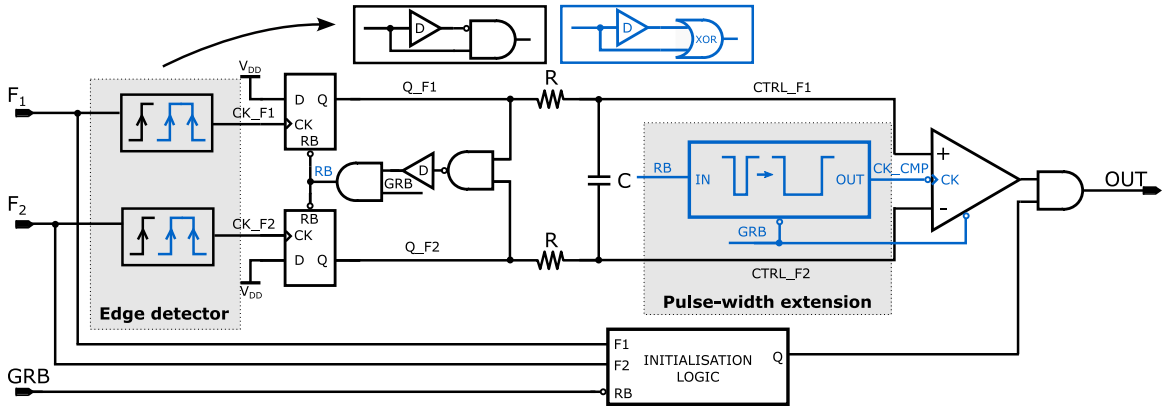

Fig. 1. Schematic diagram of the proposed FC circuit.

the phase's alignment detection logic was added. This sets a known state at the output of the FC after an initialization reset (GRB).

B. Analog comparator with hysteresis

The most important block of the proposed topology is an analog comparator with hysteresis, which is used to compare signals in the nodes $CTRL\_F1$ and $CTRL\_F2$. To obtain the widest possible input frequency range, and the capability to evaluate frequencies significantly lower than the cut-off frequency of the LPF, the analog comparator needs to have RRIO capability combined with internal hysteresis. Propagation delay and power consumption of the analog comparator have to be taken into consideration, to achieve low-power consumption of the FC as a whole. All these requirements need to be taken into account in the design phase of the analog comparator. The schematic diagram of the analog comparator used in the proposed FC is shown in Fig. 2.

In order to obtain a wide voltage range of operation, a rail-to-rail input stage was used in the designed analog comparator [5]–[7]. Therefore the NMOS input differential pair M1-M2 is connected in parallel with the PMOS input pair M3-M4. Transistors MNX and MPX were added to effectively equalize the transconductance of the combined input stage over the whole common-mode input range. Transistors M5-M6 represent the tail current sources, while diode-connected transistors M7-M10 represent the load of the NMOS and PMOS input differential pairs. The outputs of this input stage, the node $ST1_P$ and $ST1_N$, are connected to a second stage. In the second stage, labeled *Hysteresis stage* in in Fig. 2, voltage hysteresis of the analog comparator can be adjusted. Transistors M13-M14 form the differential input pair of the second (*hysteresis*) stage. The load of the second stage differential pair is a negative resistance, implemented by the use of transistors M16-M17. The voltage hysteresis can be set by the sizing of transistor M16-M19, which form a positive feedback network. To increase the output voltage swing of the analog comparator, a level translation block was employed. This block utilizes the commonly used cross-coupled voltage level shifter topology. Diode-connected transistors M26-M27 are used to limit the pull-up strength of M28-M29 and to increase the pull-down speed [8]. To limit the short-circuit current in the level shifter, transistors M30-M31 were added. A similar topology, with different input transistor arrangement, and its detailed description are presented in [9]. The last block of the designed analog comparator is a JK latch circuit. The latch is used as the evaluation stage. The JK latch uses the commonly used NAND gate architecture. Layout of the designed analog comparator, as well as of the entire FC, is shown in Fig. 3. The dimension of the designed block is 28 μm x 65 μm and thus occupy chip area of 1820 μm^2. Most of the

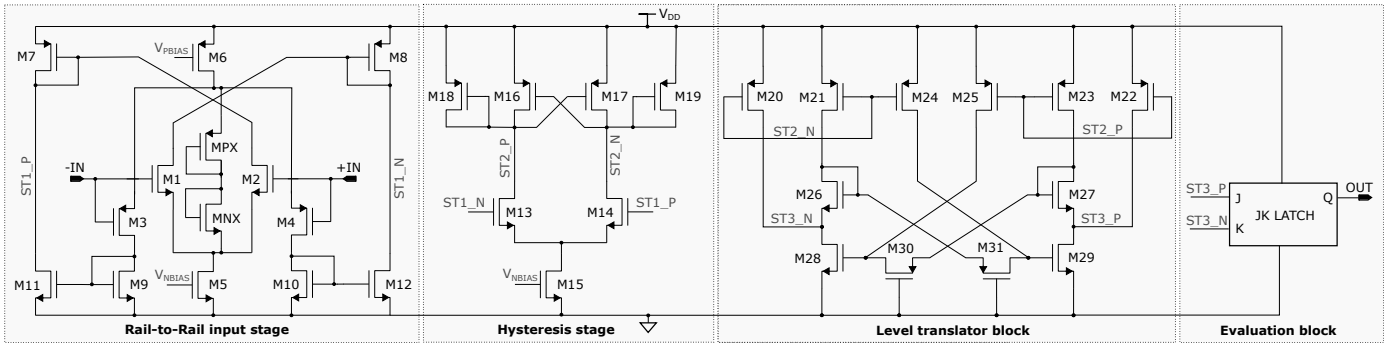

Fig. 2. Schematic diagram of the designed comparator.

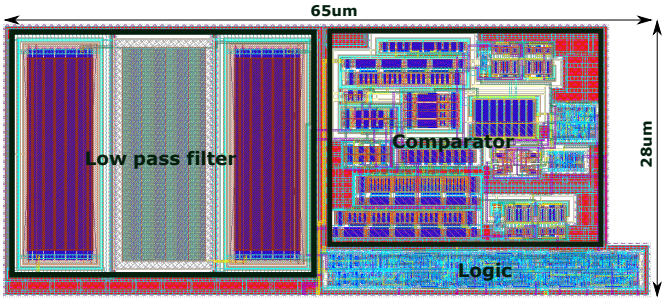

Fig. 3. The layout of proposed FC (with designed analog comparator) realized in standard UMC 65 nm CMOS process.

area is occupied by the LPF and analog comparator.

It is important to note, that instead of the analog comparator used in the proposed FC architecture, a dynamic clocked comparator (DCC) can be employed. This approach could improve some important features and decrease the overall power consumption. Such realization as well as some other improvements are discussed in the next section (Section II-C) and results are presented in Section III.

C. Possible improvements of proposed FC

Since the proposed topology of the FC is not purely digital, a disadvantage can be seen in the total power consumption. It can be especially noticeable at low input frequencies, where the static bias current of the analog comparator is the dominant source of power consumption. To further improve the power consumption of the proposed FC, a digital comparator needs to be employed. The improved FC architecture, utilizing a DCC, is highlighted in blue in Fig. 1. We used the comparator presented in [10] and shown in Fig. 4 to provide a comparison to the analog comparator. The clock signal for the DCC is generated by a pulse extension block, which uses the reset signal of the DFFs as its input. In order to increase detection speed, a XOR-based edge detector sensitive to both rising and falling edges can be used in the FC (improved FC architecture is depicted in blue in Fig. 1). This comes at the expense of increased power consumption and produces valid results only if the duty cycle of both the input and reference signals is 50%. For this reason, to ensure reliability of detection under all circumstances, using a edge detector sensitive to only one edge type is highly recommended.

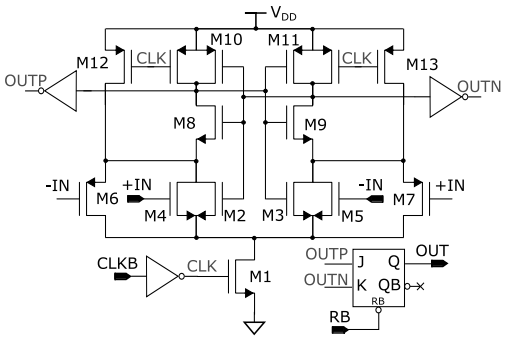

Fig. 4. Schematic of a dynamic clocked comparator presented in [10].

III. Achieved results

The results obtained by pre-layout simulation of the proposed FC and comparator are presented in this section. Fabrication process fluctuations were taken into account, and FC was simulated using Corner Analysis in the temperature range from $-20°$C to $85°$C. In these simulations F_1 is used as the input frequency ranging from $0.5F_{REF}$ to $1.5F_{REF}$ with the duty cycle of 50%. F_2 is used as the reference frequency F_{REF} with the same 50% duty cycle as F_1. The input frequency was swept with a selected slope (ramp) and the compared frequencies were in phase at the starting point of ramp, i.e. $F_1(t = 0) = 0.5F_{REF}$.

Waveforms of important circuit nodes, representing the operation of the proposed FC, are shown in Fig. 5. As can be observed, when the input frequency is higher than the reference frequency, the output goes high and vice-versa. Results in Fig. 5 have been achieved under typical condition with a ramp slope of 1000 MHz/s and the reference frequency value of 500 kHz.

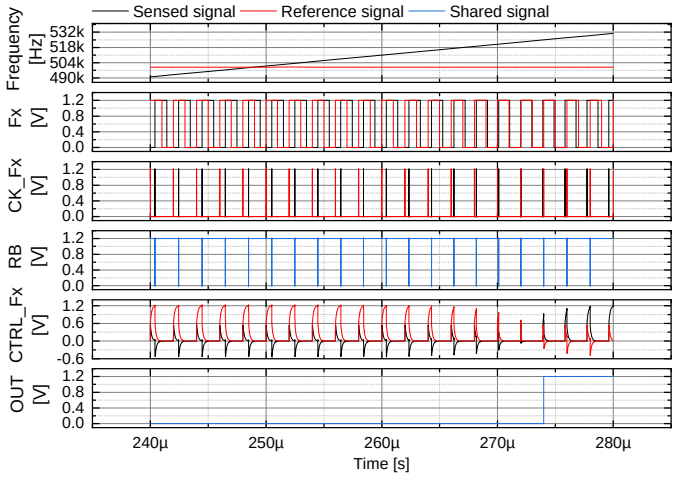

Fig. 5. Basic operation of the proposed FC, V_{DD} = 1.2 V, T = 23°C, R = 100 kΩ, C = 500 fF, F_{REF} = 500 kHz, ramp slope = 1000 MHz/s.

The investigation of frequency detection threshold dependence on LPF cut-off frequency is shown in Fig. 6. In this analysis, we consider a fixed value of capacitor (C = 500 fF in Fig. 1), while the resistor value was swept from 1 kΩ to 100 MΩ. Results were obtained for different values of the reference frequency, with the slope of the input frequency ramp changing accordingly to the reference frequency value (as described in Fig. 6). It can be observed, that the frequency thresholds are slightly above and below the reference frequency (about $\pm$ 10%) which is a result of the asynchronous nature of the signals. For low values of the LPF cut-off frequency (approaching value of F_{REF}), the frequency thresholds are shifted more apart. Therefore, the cut-off frequency of the LPF should be adjusted one decade

higher than the input and reference frequencies which are compared in FC.

Fig. 7 shows the detection delay time for different F_{REF}. It is obvious that detection delay time depends on the cut-off frequency of LPF used in the FC. It can be also observed that the detection delay time is constant for cut-off frequencies one decade higher than F_{REF}. This parameter also deviates from 25 μs to 56 μs depending on the reference frequency and ramp slopes. However, for LPF cut-off frequencies below F_{REF}, delay can be higher than 100 μs. Therefore, the LPF needs to be adjusted to higher frequencies (10x higher than F_{REF}) to improve the detection delay time of the FC circuit.

Detection delay time as well as frequency thresholds depend on the change rate of the input frequency (F_1) and phase alignment/shift at the near cross-point of the processed frequencies. In order to investigate this dependency, a ramp of the input frequency was swept with aligned 50% duty cycled signals. Simulation results of this analysis are shown in Fig. 8. Simulations were performed with the reference frequency $F_2 = F_{REF} = 250\ kHz$, while the input frequency (F_1) was swept from $0.5F_{REF}$ to $1.5F_{REF}$. A jagged behaviour without smooth trend of detection delay time dependency on the ramp slope of F_1 can be observed. Similar result was also obtained for frequency thresholds as a consequence of asynchronous nature of processed signals. On the other hand, if the slope increases, the signal's alignment (characterized by exchanging of the leading and lagging signal) is more likely to happen sooner. Therefore, the trend of detection delay time will have a declined tendency (see Fig. 5). This might be caused by evaluation mechanisms used in the proposed FC.

Another important parameter is the power consumption of the designed FC. The dependency of power consumption on the LPF cut-off frequency is shown in Fig. 9. One can conclude that the power consumption is increased for higher LPF cut-off frequencies. This is caused by the filter capacitor fully discharging/charging during each cycle. Otherwise, for

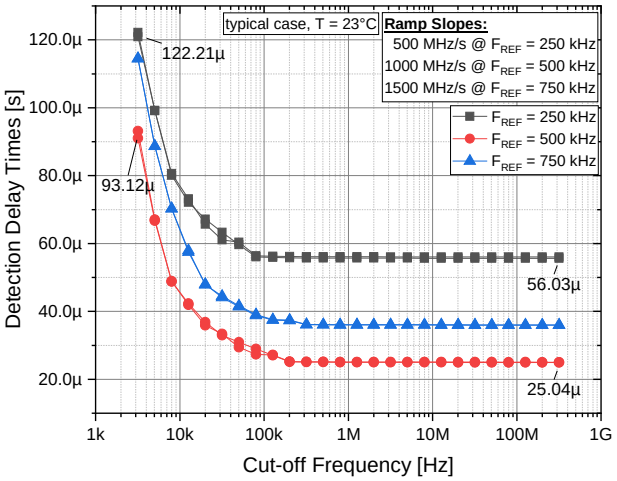

Fig. 7. Detection delay time, V_{DD} = 1.2 V, T = 23°C, C = 500 fF, R = 1 kΩ - 100 MΩ.

lower LPF cut-off frequencies, the power consumption below 1 μW can be achieved. Naturally, if $F_1 < F_2$, power consumption will be lower than in the case when $F_1 > F_2$. The power consumption will increase for higher frequencies (F_1 and F_2) being compared. Thus, for $F_2 = 750\ kHz$, the power consumption will be higher than 1.5 μW, which is still acceptable result.

Fig. 10 shows the power consumption of FC over the process corners and temperature. These results were obtained for a fixed value of LPF resistors (R = 100 kΩ, corresponding to $\approx$ 3 MHz LPF cut-off frequency). The lowest power consumption can be observed in SS corner (below 1μW), while FF corner represents the worst case scenario (2.83 μW) in terms of power consumption. In the typical corner, the power consumption of 1.05 μW was reported (for the input frequency of 250 kHz).

The main parameters of the proposed FC are summarized

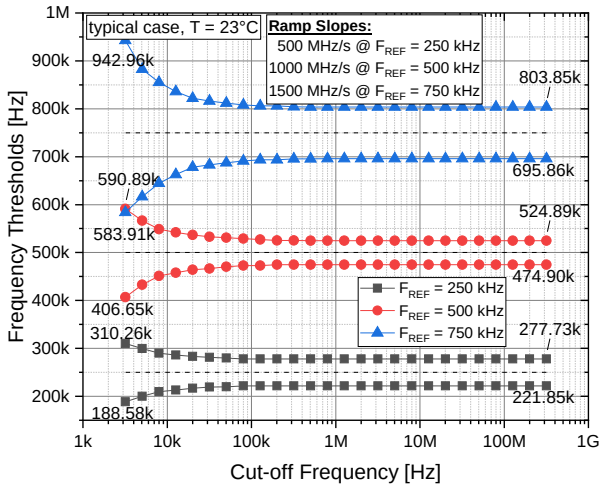

Fig. 6. Frequency detection thresholds, V_{DD} = 1.2 V, T = 23°C, C = 500 fF, R = 1 kΩ - 100 MΩ.

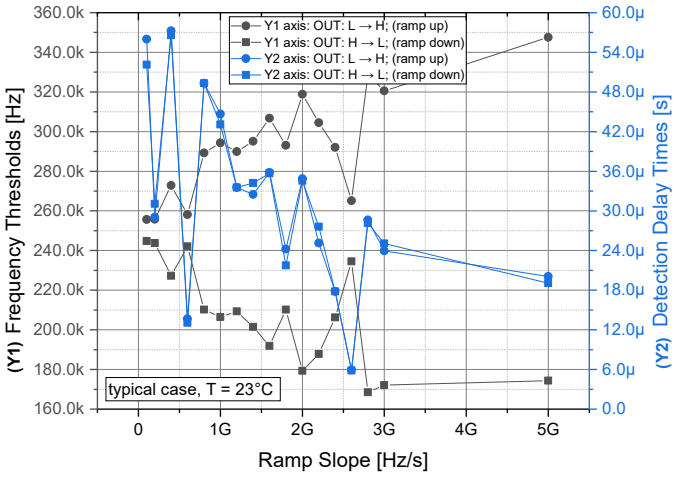

Fig. 8. Frequency thresholds and detection delay in relation to on ramp slope, V_{DD} = 1.2 V, T = 23°C, C = 500 fF, R = 100 kΩ, F_{REF} = 250 kHz.

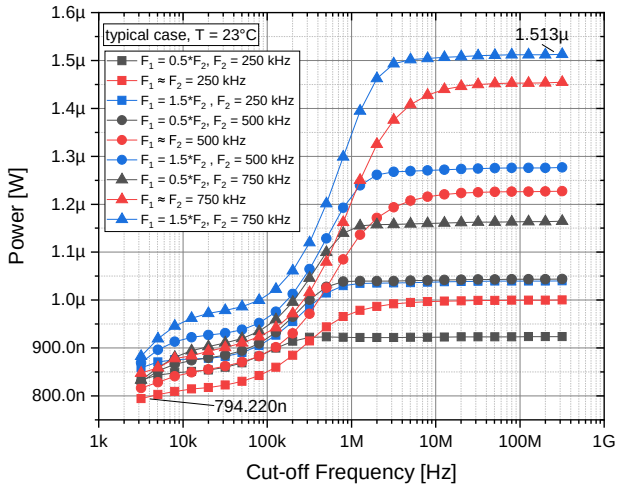

Fig. 9. Dependence of power consumption on the cut-off frequency, V_{DD} = 1.2 V, T = 23°C, C = 500 fF, R = 1 kΩ - 100 MΩ.

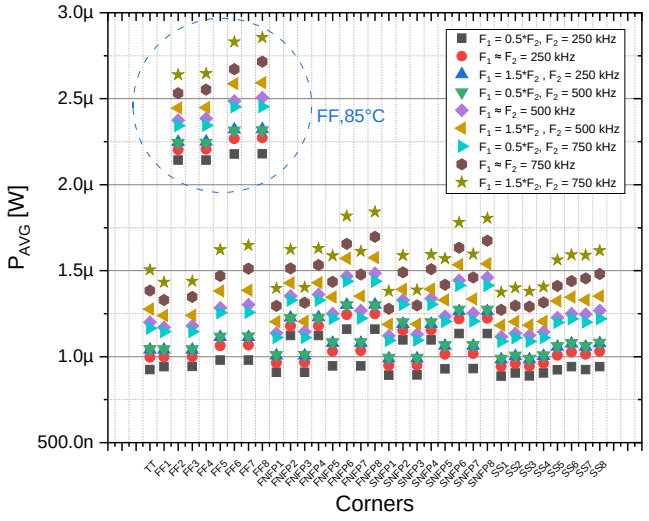

Fig. 10. Power consumption of the F circuit C over process corners, V_{DD} = 1.2 V, T = 23°C, C = 500 fF, R = 100 kΩ.

in Table I. These parameters were obtained using the reference frequency of 250 kHz. The proposed topology of FC is not sensitive to variations of process parameters, with the exception of increased mismatch in Monte Carlo analysis while the input frequency has a very low slope. This is achieved by the use of a differential topology, use of digital pre-processing circuits and the entire structure design approach. Therefore, only typical values of frequency thresholds are introduced in Table I. An exception is the power consumption, which deviates over process corners, and in the worst case, it will reach the value of 2.83 μW.

The performed observation and analysis presented above shows the efficiency of proposed FC with the designed analog comparator. However, the total power consumption is mainly caused by the static power consumption of the analog comparator. Therefore, the improved FC architecture utilizing

TABLE I
MAIN PARAMETERS OF THE PROPOSED FC

Parameter	Min	Typ	Max	Unit
Supply Voltage	-	1.2	-	V
Temperature Range	-20	27	85	°C
Total Power	0.94	1.05	2.83	μW
Frequency threshold L to H	-	277.7	-	kHz
Frequency threshold H to L	-	221.8	-	kHz
Detection Delay Time	-	56	-	μs
Area	-	1820	-	μm^2

a DCC has been proposed. This approach could outperform the previous design in terms of power consumption (for the case when comparing low frequency signals).

Fig. 11 shows signals in selected circuit nodes of the improved architecture of FC (version with DCC). The time interval around the output change is also zoomed in. This gives better understanding of the FC operation. The improved FC architecture is similar to the version with an analog comparator, except for the evaluation phase, which is triggered by the *RB* and *CK_CMP* signals. Also the frequency of pulses is doubled, due to the use of XOR-based edge detectors.

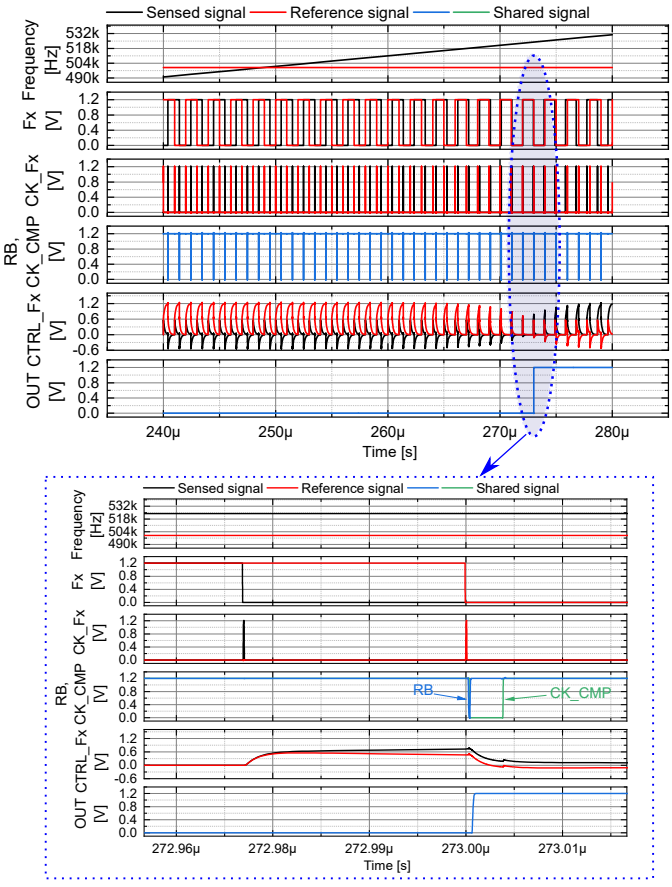

Fig. 11. Important signals of improved FC, V_{DD} = 1.2 V, T = 23°C, R = 100 kΩ, C = 500 fF, F_{REF} = 500 kHz, ramp slope = 1000 MHz/s.

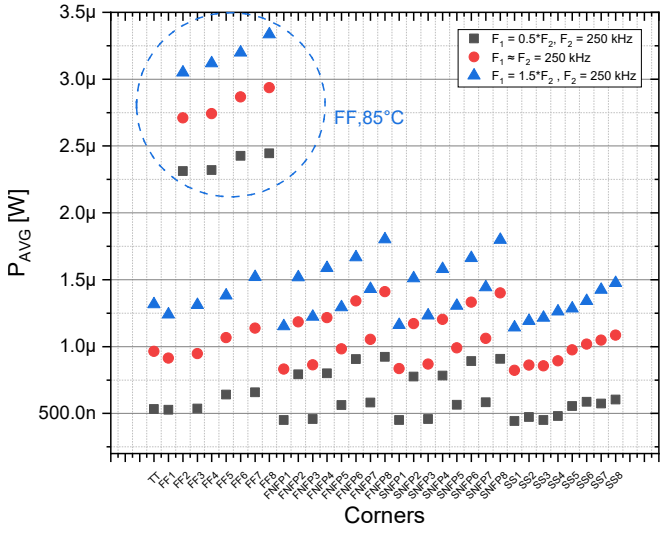

Fig. 12. Power consumption of improved FC, V_{DD} = 1.2 V, T = 23°C, C = 500 fF, R = 100 kΩ.

Fig. 12 shows the power consumption of the improved FC over the process corners and temperature. It can be observed that the improved architecture (that uses the DCC) has the power consumption of 0.53 μW in the typical case. This represents an improvement of about 50 %. On the other hand, the worst case power consumption is higher (higher than 3 μW in the FF corner) for the improved version of the FC. This is caused by the XOR-based edge detectors. As they are sensitive to both rising and falling edges, the switching frequency of the whole system is doubled, therefore the power consumption is increased in all process corners. While the XOR-based edge detectors improve speed of the FC, higher power consumption and strict 50% duty cycle of the input signals are major drawbacks and should be considered. In other words, the one-edge detector should be likely preferred for general purpose of FC and low-power applications.

IV. Conclusion

A new frequency comparator, suitable for full on-chip implementation, was designed in 65 nm CMOS technology. The proposed topology uses a RRIO analog comparator with hysteresis, which can be also replaced by a pure DCC solution to improve the overall power consumption. The proposed topology of the FC is comparatively insensitive to corner-based PVT process variations. Since the power consumption is below 2 μW (in the typical case for processed frequencies under 1 MHz), the proposed FC architecture represent an ultra low-power solution for complex mixed-signal SoC.

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