Low-Power Frequency-Locked Loop Circuit with Static Frequency Offset Cancellation

Leo Gočan*, Andro Žamboki*, Niko Bako†, Josip Mikulić†, Gregor Schatzberger†, Tomislav Marković* and Adrijan Barić*
* University of Zagreb, Faculty of Electrical Engineering and Computing, Zagreb, Croatia
† ams-OSRAM AG, Premstaetten, Austria
leo.gocan@fer.hr

***Abstract*—A phase-locked loop (PLL) is an important and commonly used electronic circuit in various electronic systems. Its main drawback is the use of an RC low-pass filter which takes up the majority of the PLL area on the chip. The RC low-pass filter is necessary to ensure the PLL stability. To mitigate this issue, a frequency-locked loop (FLL) is used because the stability of an FLL system depends on the Miller capacitance inside of the operational amplifier, which drastically reduces the capacitor size and thus the chip area. This paper presents an improved design of a fully integrated FLL. It is based on a single frequency-to-voltage converter (FVC) which uses a single capacitor and a single charging current for the frequency-to-voltage conversion of both the input and output frequencies. The use of one FVC reduces the static frequency offset caused by the mismatch between the FVCs. The circuit is implemented in a 180-nm CMOS process. The measurements show that the new FLL design has increased precision and accuracy and similar chip area compared to the previous design. It has higher power consumption, increased delay time, overshoot and settling time, but they are comparable to those of the previous design.**

***Keywords*—frequency-locked loop, frequency-to-voltage converter**

I. Introduction

A frequency-locked loop (FLL) is a circuit similar to a phase-locked loop (PLL) [1] as both circuits generate an output signal which tracks an input reference signal. The output signal of the PLL is synchronised with the input signal in phase, and therefore in frequency, whereas the output signal of the FLL is synchronised with the input signal only in frequency. The main advantage of the FLL over the PLL is a smaller die area needed to create a fully integrated circuit due to the absence of the area-consuming RC low-pass filter needed in the PLL for stabilisation.

A low-power FLL circuit with a short settling time has been reported in [2]. It is based on an FLL architecture from [3] and on a frequency-to-voltage converter (FVC) from [4] which was optimised for short settling time. Several advances in the FLL architecture based on the works [3] and [4] have been reported in [5]–[8].

This paper presents an improved design of the FLL presented in [2] in order to remove the static frequency offset caused by the mismatch between the two FVCs used in the design. Instead of the two FVCs, the FLL in this work uses a single FVC with an upgraded architecture. This results in greater accuracy and precision of the output frequency of the FLL.

This paper is organized in six sections. Section II explains the origin and the elimination of the static frequency offset caused by the mismatch between the FVCs. Section III describes the architecture and the operation of the FLL and the upgraded FVC and its control circuit. In Section IV, the measurement results of the FLL are presented. In Section V, the measurement and simulation results of the FLL from this work are compared to the measurement and simulation results of the FLL from [2]. The conclusion is given in Section VI.

II. Static Frequency Offset

A. FLL Architecture without Offset Cancellation

The measurements of the FLL design from [2] show that it exhibits a static frequency offset. The main causes of the offset are the mismatch between the two FVCs used in the design and the offset of the operational amplifier (opamp), with the former being the dominant one. In this work, the static frequency offset due to the mismatch of the two FVC circuits used in the FLL is removed.

The simplified schematic of the connection of the FVCs and the opamp from [2] is shown in Fig. 1. The two main causes of the offset are the mismatch between the charging currents I_c and $I_\mathrm{c}{}'$ and the mismatch between the capacitors C_1 and $C_1{}'$ of the FVCs because both the charging current I_c and the value of C_1 are directly related to the output voltage of the FVC through the equation [2]

$$V_{\mathrm{out,FVC}} = \frac{I_\mathrm{c}}{C_1} \cdot \frac{1}{2f_\mathrm{in}} \tag{1}$$

where f_in is the input frequency of the FVC. The capacitors C_2 and $C_2{}'$ serve only as charge storage elements, and therefore their potential mismatch does not result in any offset.

If there is a mismatch between the FVCs, in order for their output voltages to be equal, they require different input frequencies according to (1). The output voltages of the FVCs have to be equal because the opamp makes them so, thus generating a control voltage different than the one needed to generate the correct FLL output frequency. This creates the frequency offset.

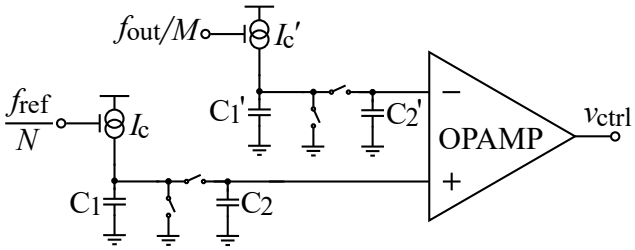

Fig. 1: The simplified schematic of the connection of the FVCs and the opamp from [2].

B. FLL Architecture with Offset Cancellation

The simplified schematic of the connection of the FVC and the opamp in this work is shown in Fig. 2. Since there is only one FVC, and since it uses a single charging current I_{c} and a single capacitor C_1, the possibility of the offset caused by the mismatch between the FVCs is removed. The capacitors $C_{2\mathrm{x}}$ and $C_{2\mathrm{y}}$ serve only as charge storage elements, and therefore their potential mismatch does not result in any offset, as it can be seen in (1).

III. Architecture and Operation

The block diagram of the proposed FLL with the static frequency offset cancellation is shown in Fig. 3. It is composed of two frequency dividers: one dividing by M and one by N, an FVC, an opamp and a voltage-controlled oscillator (VCO). The frequency dividers in this work divide by $M = 20$ and $N = 2$. The feedback loop is composed of the VCO, the frequency divider by M, the FVC and the opamp.

The operation of the FLL is as follows. The reference frequency f_{ref} is divided by N and converted into the voltage v_+ which is connected to the non-inverting input

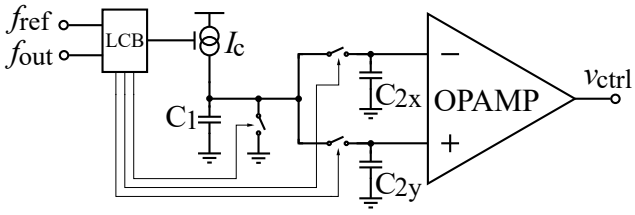

Fig. 2: The simplified schematic of the connection of the FVC and the opamp in this work.

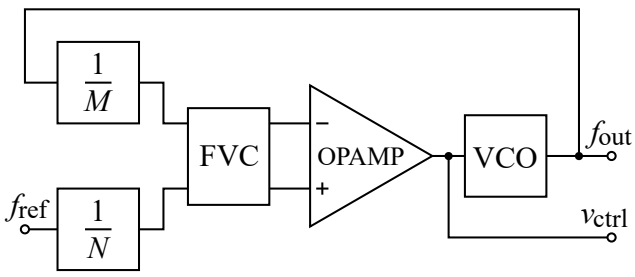

Fig. 3: The block diagram of the FLL with the static frequency offset cancellation ($M = 20$, $N = 2$).

of the opamp. The FLL output frequency f_{out}, which is also the VCO output frequency, is divided by M and converted into the voltage v_- which is connected to the inverting input of the opamp. The opamp tries to equalise the voltages at its inputs by changing its output voltage which is the control voltage v_{ctrl} of the VCO. The VCO output frequency changes until the opamp input voltages equalise. At that moment, the FLL is considered locked to the reference frequency.

The output frequency f_{out} of the FLL is defined by [2]

$$f_{\mathrm{out}} = \frac{M}{N} \cdot f_{\mathrm{ref}}. \tag{2}$$

A. Frequency-to-Voltage Converter (FVC)

The schematic of the new FVC architecture used in the offset-cancellation FLL is shown in Fig. 4. It is composed of three capacitors, a current source, several transistors that act as switches, two transmission gates with the corresponding dummy transmission gates, and a logic controller block (LCB). The dummy transmission gates are intended to compensate for the charge injection of the transmission gate. The transistors in each of them have half the width of the corresponding transistors in the transmission gate.

Unlike the former FVC architecture from [2], the new one has two distinct time intervals of conversion which alternate. During the entire first interval, the capacitor $C_{2\mathrm{y}}$ is isolated from the rest of the circuit. When the signal $F3$ goes low, the transistor MP3 turns on and the frequency f_{ref} is converted into voltage on the capacitor C_1 by means of the charging current I_{c}. When the signal $F3$ goes high, the transistor MP3 turns off, and C_1 stops charging. At the same time, $\Phi 1x$ goes high for a period of time τ_1 which turns on the transmission gate, thus connecting C_1 and $C_{2\mathrm{x}}$. The charges are redistributed between C_1 and $C_{2\mathrm{x}}$. The charge stored on the capacitor $C_{2\mathrm{x}}$ generates the voltage $v_{\mathrm{out},1}$. When the charge redistribution is finished, $\Phi 1x$ goes low, the transmission gate turns off, and $C_{2\mathrm{x}}$

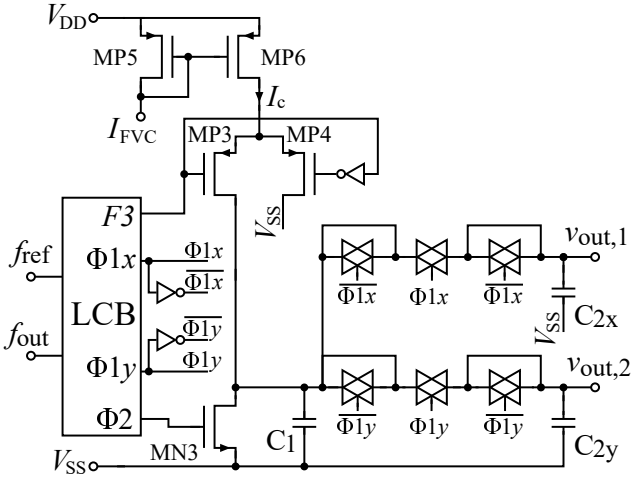

Fig. 4: The schematic of the frequency-to-voltage converter (FVC) architecture.

is isolated from the rest of the circuit. When $\Phi 1x$ goes low, $\Phi 2$ goes high for a period of time τ_2 which turns on MN3 and C_1 discharges. During the second interval, the capacitor C_{2x} is isolated from the rest of the circuit, the frequency f_{out} is converted into voltage on the capacitor C_1, and the charges are redistributed between the capacitors C_1 and C_{2y}. The charge stored on the capacitor C_{2y} generates the voltage $v_{out,2}$. Over several cycles, charges accumulate on the capacitors C_{2x} and C_{2y} and generate the voltages $v_{out,1}$ and $v_{out,2}$, respectively, which are proportional to the frequencies f_{ref} and f_{out}, respectively.

The time intervals of conversion do not have fixed values; they track the frequencies f_{ref} and f_{out} in such a way that one interval contains $N/2$ periods of the signal f_{ref} and the other interval contains $N/2$ periods of the signal f_{out}.

B. Logic Controller Block (LCB)

The new FVC architecture requires a new LCB architecture which includes an addition of an LCB controller circuit. The schematics of the new LCB architecture and of the LCB controller are shown in Figs. 5 and 6, respectively.

The LCB generates four control signals: $\Phi 1x$, $\Phi 1y$, $\Phi 2$ and $F3$, which control the elements in the FVC (Fig. 4). The signals $\Phi 1x$, $\Phi 1y$, $\Phi 2$ are pulses. The signals $\Phi 1x$, $\overline{\Phi 1x}$, $\Phi 1y$ and $\overline{\Phi 1y}$ control the transmission gates and the dummy transmission gates, the signal $\Phi 2$ controls the transistor MN3, and the signal $F3$ controls the transistors MP3 and MP4. The duration of the pulse $\Phi 1x$ must be long enough for the charge redistribution between C_1 and C_{2x} to occur. The same is applicable to the pulse $\Phi 1y$ and the capacitors C_1 and C_{2y}. The duration of the pulse $\Phi 2$ must be long enough to allow for a full discharge of C_1. The pulses $\Phi 1x$ and $\Phi 1y$ must not overlap with $\Phi 2$.

The operation of the LCB controller is as follows. When the output of the divider by N ($N = 2$ in this work) in Fig. 6 changes from 0 to 1, the SR latch SR2 is reset ($Q_2 \rightarrow 0$), and the SR latch SR1 is set ($Q_1 \rightarrow 1$) by means of a pulse synchronised with the signal f_{ref}. The pulse is generated by the circuits I0–3. With the signal Q_1 being set to 1, the NAND gate I8 generates a signal with the frequency f_{ref}, whereas with the signal Q_2 being set

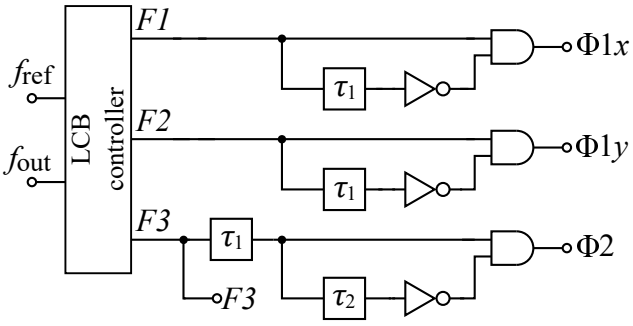

Fig. 5: The schematic of the logic controller block (LCB) architecture.

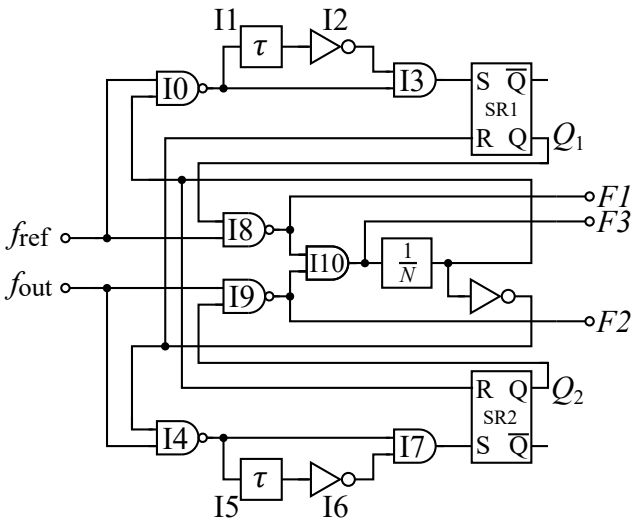

Fig. 6: The schematic of the controller for the logic controller block (LCB).

to 0, the NAND gate I9 output is held at 1. Since one of the inputs of the AND gate I10 is 1 and the other receives the signal with the frequency f_{ref}, the input of the divider by N receives the same signal. After $N/2$ periods of f_{ref}, the output of the divider by N changes from 1 to 0 and the equivalent process begins for the signal f_{out}.

The signal $F1$ contains $N/2$ periods of f_{ref}, the signal $F2$ contains $N/2$ periods of f_{out}, and the signal $F3$ is the result of the logic operation AND between $F1$ and $F2$. The signals $F1$ and $F2$ produce the signals $\Phi 1x$ and $\Phi 1y$, respectively, whereas the signal $F3$ produces the signal $\Phi 2$ and enables the charging current of the FVC.

IV. Measurement Results

The output frequency versus the reference frequency of 20 FLL chips is shown in Fig. 7. For the range of the reference frequencies from 1.5 MHz to 4 MHz, the characteristics can be considered affine, and therefore they can be approximated with lines. The slope of the lines represents the frequency multiplication factor of the FLL M/N from (2). In this work, the theoretical frequency

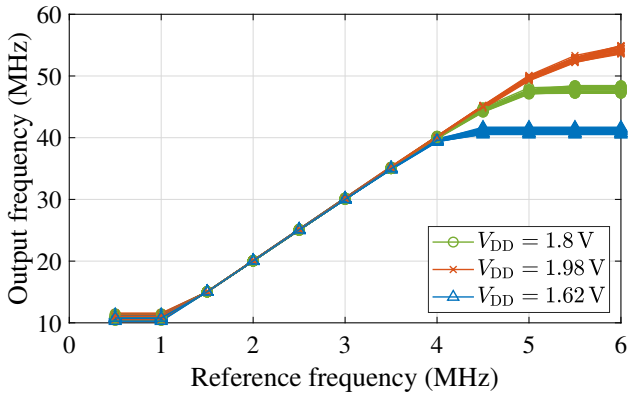

Fig. 7: The output frequency versus the input frequency of 20 FLL chips ($V_{DD} = 1.8\,V \pm 10\%$, $T = 25\,°C$).

multiplication factor is 10. For the nominal supply voltage and room temperature, the minimum slope is 9.95 and the maximum is 10.08, which is an improvement over the FLL architecture from [2] which had the minimum slope of 9.33 and the maximum of 9.94. The remaining deviation from the theoretical slope value can be reduced by eliminating the offset of the opamp. The output frequency levelling for the reference frequencies higher than 4 MHz is caused by the VCO because its output frequency levels off for sufficiently high control voltage v_{ctrl}, i.e., for sufficiently high reference frequency.

The distribution of the output frequency values of 20 FLL chips for the reference frequency of 2 MHz is shown in Fig. 8. Both the mean value of 20.04 MHz and the standard deviation of 32.79 kHz represent an improvement over the respective values of 19.22 MHz and 200.80 kHz for the FLL architecture from [2].

The period jitter and the cycle-to-cycle jitter are calculated using the definitions from JEDEC standard [9]. The period jitter is defined as the deviation in cycle time of a signal with respect to the ideal period over a number of randomly selected cycles [9]. The cycle-to-cycle jitter is defined as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs [9].

The distribution of the values of the period jitter of one FLL chip is shown in Fig. 9. The period jitter is calculated as the difference between the individual period durations and the mean period duration. The peak-to-peak jitter value is calculated using the expression

$$\text{Peak-to-peak value} = \pm 3.090 \cdot \sigma \tag{3}$$

where the value of 3.090 is taken from the Gaussian probability density function table and σ is the standard deviation. With the sample size of 1000, 999 samples will, on average, fall within $\pm 3.090\sigma$ from the mean value. Both the standard deviation of 0.38 ns and the peak-to-peak jitter value of ± 1.18 ns represent an improvement over the respective values of 0.62 ns and ± 1.92 ns for the FLL architecture from [2].

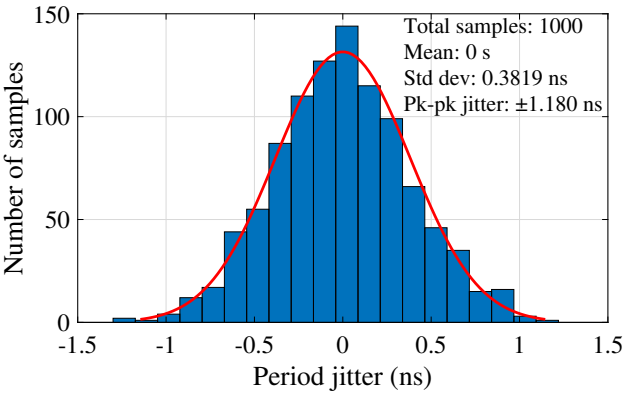

Fig. 9: The distribution of the values of the period jitter of one FLL chip ($V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $T = 25\,^{\circ}\mathrm{C}$, $f_{\mathrm{ref}} = 2\,\mathrm{MHz}$).

The distribution of the values of the cycle-to-cycle jitter of one FLL chip is shown in Fig. 10. The cycle-to-cycle jitter is calculated as the difference between the durations of every two adjacent periods. Both the standard deviation of 0.65 ns and the peak jitter value of 2.46 ns represent an improvement over the respective values of 1.07 ns and 3.89 ns for the FLL architecture from [2].

The reduction of the period jitter and the cycle-to-cycle jitter is a result of the use of a single charging current source and a single capacitor C_1 in the FVC (see Fig. 4). They are the critical analogue elements, and their mismatch increases the jitter, but by removing the possibility of the mismatch, the jitter is reduced.

V. Comparison with Previous Work

The comparison of the typical values of the parameters of both FLL designs is shown in Table I. The mean value and the standard deviation of the output frequency are improved in the new design, but the power consumption and the 0.1-% settling time are degraded. The new design has a marginally increased area which is still significantly

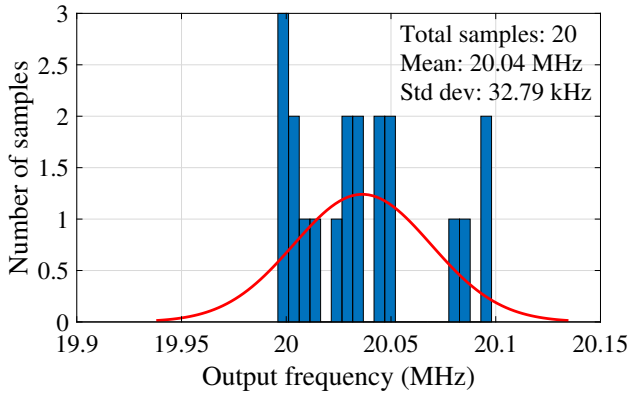

Fig. 8: The distribution of the output frequency values of 20 FLL chips for the reference frequency of 2 MHz ($V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $T = 25\,^{\circ}\mathrm{C}$).

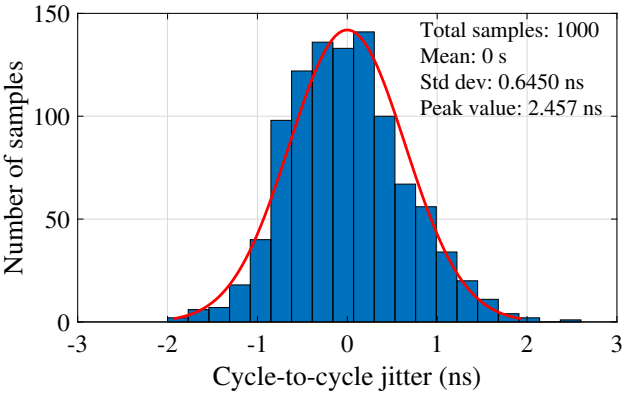

Fig. 10: The distribution of the values of the cycle-to-cycle jitter of one FLL chip ($V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $T = 25\,^{\circ}\mathrm{C}$, $f_{\mathrm{ref}} = 2\,\mathrm{MHz}$).

TABLE I: The measured typical values of the parameters of both FLL designs ($V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $T = 25\,^{\circ}\mathrm{C}$, $f_{\mathrm{ref}} = 2\,\mathrm{MHz}$). The sample size for the old design is 10 chips and for the new one is 20 chips.

Parameter	Unit	Old FLL design [2]	New FLL design
f_{out} mean	MHz	19.22	20.04
f_{out} std. dev.	kHz	200.80	32.79
I_{DD}	µA	91.85	111.13
Power consumption	µW	165.33	200.03
0.1-% settling time	µs	13.36	20.54
Area	$\mu\mathrm{m}^2$	40 998	41 535

smaller than the area of a PLL with the same output frequency.

The extreme values of the simulated transient parameters of both FLL designs across technology corners are shown in Table II. The simulation was conducted from a steady state by changing the reference frequency f_{ref} from $2\,\mathrm{MHz}$ to $2.1\,\mathrm{MHz}$. The degradation of the transient parameters in the new FLL design is due to the use of a single FVC in which the charge redistribution step for each FVC output voltage must wait for the previous charge redistribution step to finish, and therefore the opamp input voltages are generated alternately. Conversely, the FVCs in the FLL design from [2] allowed for an independent and simultaneous generation of the opamp input voltages. This resulted in an overall faster circuit compared to the FLL design in this work.

The comparison of the output frequencies of both FLL designs for different temperatures is shown in Table III. The output frequency of the old FLL design is temperature dependent, whereas the output frequency of the new FLL design shows no significant temperature dependence. The temperature coefficient of the output frequency is $4839\,\mathrm{Hz}/^{\circ}\mathrm{C}$ for the old FLL design and $-91.9\,\mathrm{Hz}/^{\circ}\mathrm{C}$ for the new one.

The current consumption of both FLL designs for different temperatures is shown in Table IV. The current consumption of the new FLL design is larger than the current consumption of the old FLL design. The temperature coefficient of the supply current is $38\,\mathrm{nA}/^{\circ}\mathrm{C}$ for the old FLL design and $147\,\mathrm{nA}/^{\circ}\mathrm{C}$ for the new one.

TABLE II: The extreme values of the simulated transient parameters of both FLL designs across technology corners ($f_{\mathrm{ref}}: 2\,\mathrm{MHz} \rightarrow 2.1\,\mathrm{MHz}$).

Parameter		Old FLL design [2]	New FLL design
Delay	Min	1.2	5.0
(µs)	Max	10.7	18.7
0.1-% settling time	Min	10.7	20.5
(µs)	Max	58.3	77.7
Overshoot (% of steady state)	Max	1	1.19

TABLE III: The measured output frequencies of both FLL designs for different temperatures ($V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $f_{\mathrm{ref}} = 2\,\mathrm{MHz}$). The sample size for the old design is 10 chips and for the new one is 20 chips.

	Output frequency (MHz)	
Temperature (°C)	Old FLL design [2]	New FLL design
−40	18.84 ± 0.27	20.06 ± 0.04
25	19.22 ± 0.20	20.04 ± 0.03
75	19.39 ± 0.17	20.05 ± 0.03

TABLE IV: The measured current consumption of both FLL designs for different temperatures ($V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $f_{\mathrm{ref}} = 2\,\mathrm{MHz}$). The sample size for the old design is 10 chips and for the new one is 20 chips.

	Supply current (µA)	
Temperature (°C)	Old FLL design [2]	New FLL design
−40	89.34 ± 1.36	99.97 ± 1.07
25	91.85 ± 1.09	111.13 ± 1.65
75	93.71 ± 1.05	116.76 ± 0.98

VI. Conclusion

This paper presents an improved design of a frequency-locked loop (FLL) circuit from [2] which suffered from a static frequency offset caused by the mismatch between the frequency-to-voltage converters (FVC). The FLL design in this work uses a single FVC with an upgraded architecture, thus eliminating the aforementioned static frequency offset. The circuit is implemented in a 180-nm CMOS process. The measurement results show that the output frequency of the FLL design from this work is more accurate and more precise than that of the design from [2]. The measurements also show that the new FLL design has an increased power consumption compared to the old one. The simulation results show that the delay, the 0.1-% settling time and the overshoot are increased for the new FLL design. The area of the new FLL design is marginally increased.

Acknowledgment

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