Stress-dependent MOSFET Model for use in Circuit Simulations

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***Abstract*—This paper presents a stress-dependent MOSFET model based on existing transistor models. The encapsulation of chips is often made from polymers (such as epoxy) which are poured over the silicon chips. When the encapsulation cools, it generates a significant amount of static mechanical stress in the ICs which changes their performance. To compensate for the offsets caused by the stress, chip designers need to be able to simulate the effects of stress on their circuits and design stress sensors and active stress-compensating circuits. In this paper, a stress-dependent MOSFET model is implemented by combining existing transistor models and a Verilog-A cell. In this way, temperature, corner and other transistor variations can be simulated in combination with stress. Simulations show that this model can be used to simulate the stress effects on circuits and to design and optimize stress-compensating circuits.**

***Keywords*—stress, MOSFET model, SPICE simulation, optimization, stress compensation, encapsulation**

I. INTRODUCTION

THE stress caused by integrated circuit (IC) packaging has been thoroughly studied in literature [1] [2] [3]. During the IC packaging process, a significant amount of static stress that varies with temperature can be introduced by the encapsulation to the surface of the silicon. These stresses can have values higher than 100 MPa [3]. It has been shown extensively that this induced stress has a detrimental impact on circuits, especially biasing sources and oscillators [2] [4].

To analyze and compensate these stress-induced effects, researchers have designed stress sensors, complex stress sensing circuits and active stress offset-canceling subcircuits but, often, circuit simulators do not have an easy way of simulating the stress-induced effects on circuits. In [5] authors propose a Verilog-A stress upgrade for the PSP MOSFET model with the focus on highly flexible thin silicon chips. In [4] authors propose a statistical model focused on reference circuits. A more generalized model is needed that can be applied to different types of MOS silicon technologies that circuit designers use and which can be easily implemented, customized and improved.

In Section II the basics of the semiconductor stress theory are shown. In Section III a model calibration technique is laid out. In Section IV we propose stress-enhanced add-ons which can be attached to the existing MOSFET or resistor models. Simulations in Section V show that these models perform well in designing and testing stress sensors and identifying the most stress-sensitive parts of the circuits. It is also shown in Section V that this sensitivity can be reduced by changing the orientation of the transistors. Section VI presents conclusions.

II. THEORETICAL BASICS

To create a MOSFET stress model for use in circuit simulations, an analysis has to be done of the impacts of stress on transistors. The analysis in this paper uses the wafer coordinate system shown in Fig. 1 where it is assumed that the silicon wafer is (100) type. For (111) wafer types, the analysis gets somewhat more complicated but the overall procedure remains the same [6].

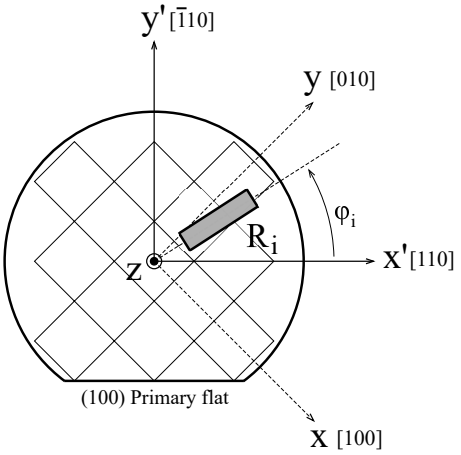


Fig. 1: Wafer coordinate system. The rectangular grid in the wafer represents the silicon crystal lattice orientation.

The change in the MOSFET drain current due to the mechanical stress is described by the following relation:

$$I_D = I_{D0} + \Delta I_D = I_{D0}\left(1 + \frac{\Delta I_D}{I_{D0}}\right) \tag{1a}$$

where I_{D0} is the unstressed MOSFET current in the linear region:

$$I_{D0} = K\left(U_{GS} - U_{GS0} - \frac{U_{DS}}{2}\right)U_{DS} \tag{1b}$$

or in the saturation region:

$$I_{D0} = \frac{K}{2}(U_{GS} - U_{GS0})^2 \tag{1c}$$

where K is the current coefficient of the MOSFET:

$$K = \mu C'_{OX} \frac{W}{L} \tag{1d}$$

where μ is the carrier mobility, C'_{OX} is the thin-oxide capacitance per unit area and W and L are the transistor width and length. It can be seen in (1) that the change of the MOSFET drain current ΔI_D because of the stress can be due to the carrier mobility μ variation, transistor dimensions W/L variation and/or threshold voltage U_{GS0} variation. Extensive research has been done on the magnitudes of these effects on the MOSFET current and the overall consensus in literature is that the impact of the carrier mobility variation vastly outweighs all other variations [7] in the strong inversion. Stress-dependent threshold shifts significantly alter the stress responses in moderate and weak inversion [1]. Regardless of the operating region, the proposed MOSFET stress model can still be used to simulate approximate stressed states in circuits and for stress-optimized circuit design.

So by neglecting all other variations, the change in the MOSFET current due to the stress can be directly linked with the change in the carrier mobility:

$$\frac{\Delta I_D}{I_{D0}} \approxeq \frac{\Delta \mu}{\mu}. \tag{2}$$

The resistance of a material is defined by:

$$R(\mu) = \frac{1}{\mu} \frac{L}{qntW} \tag{3}$$

where q is the elementary charge, n is the charge density and the t, W and L are the height, width and length of the material respectively. So the change of the material resistance (in this case, the MOSFET channel resistance) due to the change in the carrier mobility is:

$$\frac{\Delta R}{R} = \frac{R(\mu) - R(\mu_0)}{R(\mu_0)} = -\frac{\mu - \mu_0}{\mu} = -\frac{\Delta \mu}{\mu}. \tag{4}$$

By combining (1a), (2) and (4), the final equation for modeling the transistor behavior with respect to stress is extracted:

$$I_D = I_{D0} \left(1 - \frac{\Delta R}{R}\right). \tag{5}$$

The change of the MOSFET channel resistance $\Delta R/R$ due to stress is described by (6) [7]:

$$\begin{aligned} \frac{\Delta R}{R} = &\left[\frac{\pi_S + \pi_{44}}{2}\sigma'_{11} + \frac{\pi_S - \pi_{44}}{2}\sigma'_{22}\right]\cos^2\varphi \\ &+ \left[\frac{\pi_S - \pi_{44}}{2}\sigma'_{11} + \frac{\pi_S + \pi_{44}}{2}\sigma'_{22}\right]\sin^2\varphi \\ &+ \pi_D \sigma'_{12} \sin 2\varphi + f(T) \end{aligned} \tag{6a}$$

where function $f(T)$ models the temperature dependence of the resistance:

$$f(T) = \alpha_1 T + \alpha_2 T^2 + \alpha_3 T^3 \cdots. \tag{6b}$$

The coefficients $\pi_S = \pi_{11} + \pi_{12}$, $\pi_D = \pi_{11} - \pi_{12}$, π_{11}, π_{12} and π_{44} are the piezoresistive coefficients. They are the characteristics of the material in which integrated components are made. Equation (6a) is standard in literature and describes the change of the resistance of a material as a function of normal stresses σ'_{11} and σ'_{22} and shear stress σ'_{12}. The component σ'_{11} is the stress in the x' (Fig. 1) direction acting on a plane with a normal in the x' direction. Likewise, σ'_{22} is the stress in the y' direction acting on a plane with a normal in the y' direction. The value σ'_{12} is the stress in the y' direction acting on a plane with a normal in the x' direction. The angle φ is the direction of the current through the resistance shown in Fig. 1 (counterclockwise rotation has positive angles). Some standard values for lightly doped silicon are shown in Table I. For the greatest match in behaviour under stress between the modeled and manufactured MOSFETs, piezoresistive coefficients should be measured for the silicon technology the circuit designer is using.

TABLE I: Typical piezoresistive coefficient values for lightly doped silicon TPa^{-1} [1].

	n-type silicon	p-type silicon
π_{11}	-1022	66
π_{12}	534	-11
π_{44}	-136	1381

III. MODEL CALIBRATION

Although the approximate circuit behaviour can be simulated with the stress MOSFET models using the coefficients in Table I, to get more accurate results, a piezoresistive coefficient extraction for the used silicon technology should be done. Since (6) depends on π_S, π_D, and π_{44}, these values have to be measured. To get accurate results, these coefficients should be temperature compensated. In [8] authors use simple methods for calibration but π_S and π_D are not temperature compensated so the temperature during measurement has to be precisely controlled. To mitigate this issue, we use the more complex off-axis rosette MOSFET sensor for calibration [9].

The off-axis rosette is constructed by creating a coordinate system $x'' - y''$ which is rotated by θ (considered as a positive angle as drawn in Fig. 2) in the $x' - y'$ plane. Then placing 3 transistors in three directions: first in the x'' direction, second in the y'' and third in the direction that is rotated 45° counterclockwise from the direction x''. The off-axis rosette design is shown in Fig. 2.

Next, to analyze the current through the off-axis rosette transistors using (5), a coordinate system shift from $x' - y'$ to $x'' - y''$ is done. The stress vectors σ_{jk} are transformed using the matrix rotation operation in (7) [9]:

$$\begin{bmatrix} \sigma''_{11} \\ \sigma''_{22} \\ \sigma''_{12} \end{bmatrix} = \begin{bmatrix} \cos^2\theta & \sin^2\theta & -2\sin\theta\cos\theta \\ \sin^2\theta & \cos^2\theta & 2\sin\theta\cos\theta \\ \sin\theta\cos\theta & -\sin\theta\cos\theta & \cos^2\theta - \sin^2\theta \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{22} \\ \sigma'_{12} \end{bmatrix} \tag{7a}$$

and written with matrix symbols:

$$\boldsymbol{\sigma}'' = \boldsymbol{R}\boldsymbol{\sigma}'. \tag{7b}$$

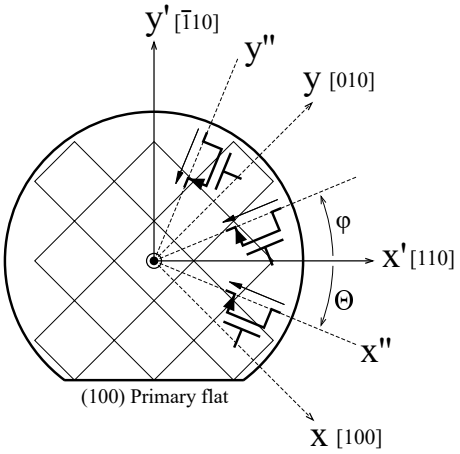


Fig. 2: Off-axis rosette wafer coordinate system.

By substituting σ'_{jk} with σ''_{jk} in (6) and calculating the results for the angle φ of the three off-axis transistors: $\varphi_1 = -\theta$, $\varphi_2 = -\theta + 45°$ and $\varphi_3 = -\theta + 90°$, the $\Delta R_i/R_i$ expressions can be derived for the transistors. If the piezoresistive coefficients are extracted from the calculated $\Delta R_i/R_i$ and if the uniaxial stress is applied in the y'' direction $\sigma''_{22} = \sigma$ ($\sigma''_{11} = \sigma''_{12} = 0$), the following expression can be derived:

$$\begin{bmatrix} \Delta R_1/R_1 \\ \Delta R_2/R_2 \\ \Delta R_3/R_3 \end{bmatrix} = \boldsymbol{C} \begin{bmatrix} \pi_{11} \\ \pi_{12} \\ \pi_{44} \end{bmatrix} \cdot \sigma \tag{8}$$

where $\boldsymbol{C}$ is the coefficient matrix which will be explained later. For the calibration, only the stress in one direction is needed. Calibrating the model by generating the stresses σ''_{11} and σ''_{22} should yield the same piezoresistive coefficients. Combining (2), (4) and (8) we get:

$$\begin{bmatrix} \Delta I_{D1}/I_{D0} \\ \Delta I_{D2}/I_{D0} \\ \Delta I_{D3}/I_{D0} \end{bmatrix} = -\boldsymbol{C} \begin{bmatrix} \pi_{11} \\ \pi_{12} \\ \pi_{44} \end{bmatrix} \cdot \sigma = \boldsymbol{k} \cdot \sigma \tag{9}$$

where the matrix $\boldsymbol{k}$ represents the slopes of the $\Delta I_{Di}/I_{D0}$ vs. σ graphs:

$$\boldsymbol{k} = -\boldsymbol{C} \cdot \boldsymbol{\pi}. \tag{10}$$

By rearranging (10), the piezoresistive coefficients can be calculated from the normalized MOSFET current change vs. stress graph slopes:

$$\begin{bmatrix} \pi_{11} \\ \pi_{12} \\ \pi_{44} \\ \pi_D \end{bmatrix} = -\boldsymbol{D} \begin{bmatrix} k_1 \\ k_2 \\ k_3 \end{bmatrix} \tag{11}$$

where the index i in k_i denotes the respective MOSFET for which k is measured. $\boldsymbol{D} = \boldsymbol{C}^{-1}$ with the added fourth row. This row is constructed by subtracting the first and second rows of $\boldsymbol{D}$ (π_D = π_{11} - π_{12}). The generalized form of $\boldsymbol{D}$ is shown in (12a):

$$\boldsymbol{D} = \begin{bmatrix} -\frac{2\cos^2\theta - 1}{4A} & \frac{2\cos^2\theta - 1}{2A} & \frac{4A - 2\cos^2\theta + 1}{4A} \\ \frac{4A + 2\cos^2\theta - 1}{4A} & -\frac{2\cos^2\theta - 1}{2A} & \frac{2\cos^2\theta - 1}{4A} \\ -\frac{\cos 2\theta - \sin 2\theta}{\cos 2\theta} & -\frac{2\sin 2\theta}{\cos 2\theta} & \frac{\cos 2\theta + \sin 2\theta}{\cos 2\theta} \\ -\frac{2\cos^2\theta - 1 + 2A}{2A} & \frac{2\cos^2\theta - 1}{A} & -\frac{2\cos^2\theta - 1 - 2A}{2A} \end{bmatrix} \tag{12a}$$

where

$$A = \cos\theta \sin\theta. \tag{12b}$$

The final procedure is then constructed for the stress MOSFET model calibration:

1) Design an off-axis rosette with an angle of $\theta = <0°, 45°>$ (excluding $0°$ and $45°$).
2) Cut a long silicon stripe in the y'' direction with the rosette in the middle and apply a controlled stress using the four-point bending stress test [10].
3) Calculate the $\boldsymbol{D}$ matrix for the chosen angle θ.
4) Measure the $\Delta I_{Di}/I_{D0}$ for a range of stress values σ and extract the graph slopes k_i using the least squares method for the three transistors.
5) Calculate the piezoresistive coefficients with the measured k_i values using (11).

Equation (13) shows the matrix $\boldsymbol{D}$ if the angle θ is chosen to be 22.5°:

$$\boldsymbol{D}|_{\theta=22.5°} \begin{bmatrix} -0.5 & 1 & 0.5 \\ 1.5 & -1 & 0.5 \\ 0 & -2 & 2 \\ -2 & 2 & 0 \end{bmatrix}. \tag{13}$$

By analyzing the generalized form of the matrix $\boldsymbol{D}$, it can be observed that the third and fourth rows always add up to 0 regardless of the angle θ. If it is assumed that the temperature impacts all k_i values in an identical way (the temperature characteristics of transistors are expected not to depend on their direction), then the π_{44} and π_D measurements should be temperature compensated. Consequently, π_{11} and π_{12} are not temperature compensated. Since π_S is the sum of π_{11} and π_{12}, their temperature dependence will also be summed. Therefore, π_S is not temperature compensated. Alternatively, this coefficient can be estimated from $\pi_D = 3\pi_S$ based upon well-known theoretical results for electrons in silicon ($\pi_{11} = -2\pi_{12}$) [8]. Since, π_D is temperature compensated, π_S will be as well.

Using this method the piezoresistive coefficients have to be extracted for both nMOS and pMOS transistors as well as for all other used silicon devices (e.g. if resistors are used, then an off-axis resistor rosette has to be constructed and $\Delta R_i/R_i$ measurements have to be taken). For more precise measurements, the frequency method, the laser interferometer technique and the quasi-static method may be used [11].

IV. STRESS MOSFET MODEL

As stated before in (5), the current through a MOSFET transistor under mechanical stress is described by the following expression:

$$I_D = I_{D0} - I_{D0}\frac{\Delta R}{R} \tag{14}$$

where $\Delta R/R$ is the transistor channel resistance change due to stress and is described by (6). The problem with modeling the impact of stress on the transistor current is that the channel resistance is impacted by the carrier mobility variation but, in most cases (including this one), the only transistor parameters that can be changed are the channel dimensions W and L. So a stress-dependent transistor model has to be created around the existing stress-invariant MOS transistors. Fig. 3 shows a model that mimics (14). It works in the following way: a black box is created like the one in Fig. 3. A Verilog-A model is written to create an ideal current source which measures the current through the transistor I_{D0} and generates a current equal to $I_{D0}\cdot\Delta R/R$ and is parallel to the transistor. This current source calculates $\Delta R/R$ and is controlled by the voltages $U_{\sigma 11'}$, $U_{\sigma 22'}$ and $U_{\sigma 12'}$, which correspond to the values of the stresses σ'_{11}, σ'_{22} and σ'_{12} (1 V is equivalent to 1 Pa). A user defined value of φ (in degrees) determines the direction of the transistor relative to the x' direction. By analyzing this model, the following equations can be extracted:

$$I_X + I_{D0}\frac{\Delta R}{R} = I_{D0} \tag{15a}$$

$$I_Y + I_{D0}\frac{\Delta R}{R} = I_{D0}. \tag{15b}$$

So from the outside of the black box the following currents are measured:

$$I_X = I_Y = I_{D0} - I_{D0}\frac{\Delta R}{R}. \tag{16}$$

I_X and I_Y are identical to (14) which means that the black box will act like a transistor under mechanical stress and its current will change accordingly. This black box can be made as a new component which has φ and the transistor dimensions W and L set as user-editable variables. In this way, stress simulations can easily be incorporated into existing circuits by replacing the stress-invariant MOSFET models with the stress-dependent models.

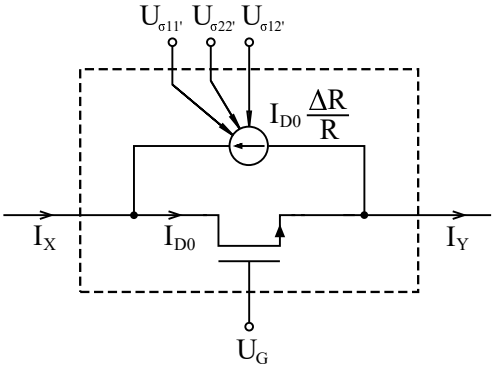
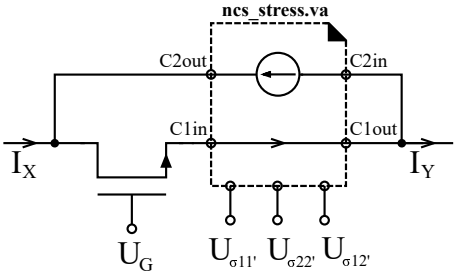
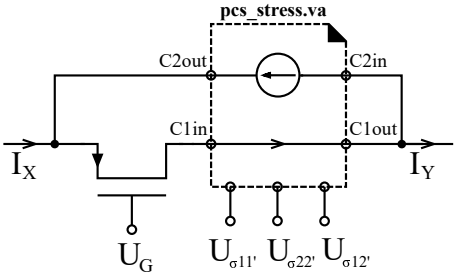


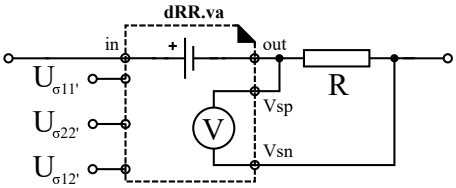
Fig. 3: Stress-dependent MOSFET model which can be implemented using Verilog-A.



(a) nMOS transistor model.



(b) pMOS transistor model.

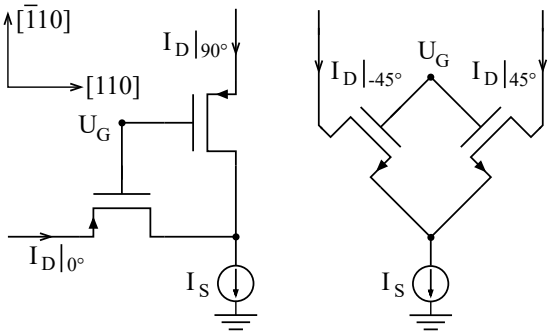


(c) Resistor model.

Fig. 4: Verilog-A implementation of the stress-dependent transistor and resistor models.

The biggest advantage of using this model is that all nonlinearities, temperature and corner variations of the transistor model are kept in I_{D0}. The transistor stress-dependent model can be simulated for temperature and corner variations the same way one would do for a standard transistor model. This model can be used for both pMOS and nMOS transistors.

Fig. 4a shows how the stress-dependent nMOSFET model is implemented. A current controlled current source written in Verilog-A (code in Appendix A) measures the current through the ports $C1in - C1out$, multiplies it by $\Delta R/R$ and forces that current through the ports $C2in - C2out$. $\Delta R/R$ is calculated using the input control voltages $U_{\sigma 11'}$, $U_{\sigma 22'}$ and $U_{\sigma 12'}$ and the CDF parameter phi (φ). This parameter is set up to allow the user to set a custom angle value for each stress-dependent transistor. The same model can be made with a pMOS transistor but the piezoresistive coefficients in the Verilog-A code have to substituted for those of the p-type silicon. Using these models, a comprehensive stress analysis can be made on CMOS circuits. By using global control voltages for σ_{jk}, the stress magnitude and direction can be dynamically altered. A chip designer can then pinpoint the critical circuit parts that are sensitive to stress.



(a) Normal stress pMOS sensor.

(b) Shear stress nMOS sensor.

Fig. 5: Differential pair MOSFET stress sensors.

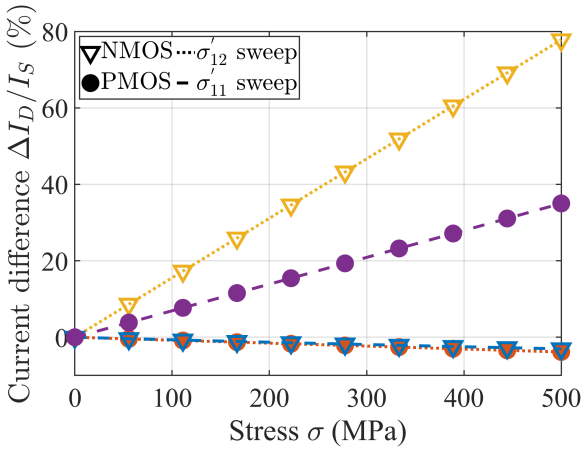


Fig. 6: Normalized current differences of MOSFET differential pairs in Fig. 5 in response to a stress sweep. Dotted and dashed lines represent the σ'_{12} and σ'_{11} stress sweeps respectively. The triangles and circles represent nMOS and pMOS sensors respectively.

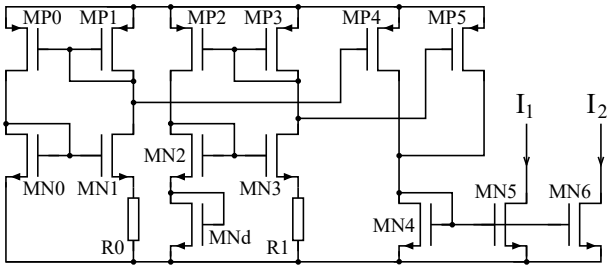


Fig. 7: CMOS reference current source.

To make this model user-friendly in Cadence Virtuoso, the adjustments which are described in Appendix B should be performed. This will enable the circuit designer to change the length, width and direction of each stress MOSFET instance separately in an identical way it would be done for a regular transistor circuit model.

The methodology of creating a stress model shown in this chapter can also be applied on resistors. In that case, the model in Fig. 4c is used. The Verilog-A block $dRR.va$ is similar to $ncs\_stress.va$ but with a different analog block:

```
analog begin
      V(in,out) <+ ΔR/R *V(Vsp,Vsn);
end
```

where $\Delta R/R$ is shown in (6). In short, this model mimics the added voltage drop on a resistor due to the change of the resistance ΔR caused by the stress.

V. USE CASES AND EXAMPLES

The stress MOSFET model can be used to design and calibrate new stress sensors. The following examples use the 180-nm CMOS technology node and the piezoresistive coefficients from literature shown in Table I. Fig. 5 shows the normal stress pMOS sensor (Fig. 5a) and a shear nMOS sensor (Fig. 5b). In literature, it is accepted that the normal stress sensors are less sensitive to shear and should be made from pMOSFETs due to their increased sensitivity to normal stress [7]. Likewise, the shear sensors are less sensitive to normal stress and should be made from nMOSFETs due to their increased sensitivity to shear. To test this fact, a schematic is made where normal stress and shear sensors are made from both pMOS and nMOS transistors. Then the normal stress σ'_{11} and shear σ'_{12} are swept separately and the sensor currents are plotted in Fig. 6. It can be clearly seen that the slope (sensitivity) of the pMOS normal stress sensor is larger then that of the nMOS normal stress sensor. The opposite is true for the shear stress sensors.

The models presented in this work can also be used to analyze the impact of stress on more complicated circuits. In that case, the parts of the circuit that are most sensitive to stress can be identified. The example in Fig. 7 shows a schematic of a standard temperature-invariant CMOS reference current source. It is designed so that the output reference currents are: I_1 = 1 µA and I_2 = 4 µA. The simulation results in Fig. 8a show the change of the output reference currents when all elements are at an angle of φ = 0°. The output currents are sensitive to normal stresses σ'_{11} and σ'_{22} (but are less sensitive to shear σ'_{12}). In the worst case, the absolute output current sensitivity is 16.4 %/GPa. Fig. 8b shows the change of the output reference currents when the transistors MP4 and MP5 are both rotated by φ = 25°. With this modification, the worst case absolute output current sensitivity is 6.0 %/GPa. By changing the angle of just two transistors, the reference current source has been improved.

VI. CONCLUSION

This paper presents a stress-dependent MOSFET and resistor models that can be easily fitted around existing models. These models can be used by circuit designers to simulate the effects of stress caused by packaging on their circuits. A detailed procedure for calibrating the models is presented so that the simulations best represent the behaviour under stress of the used silicon technologies. For approximate simulation results, previously measured silicon piezoresistive coefficients can also be used without the need for model calibration. Simulations show that the

models can be used for stress sensor design/optimization, to decrease the reference source sensitivity to stress and to design active subcircuits that minimize the offsets caused by stress.

APPENDIX A
CURRENT CONTROLLED CURRENT SOURCE VERILOG-A CODE *ncs_stress.va* FROM FIG. 4A

```
`include "constants.vams"
`include "disciplines.vams"
module ncs_stress(C2in,C2out,C1in,C1out
    ↪ ,O11,O22,O12);
       electrical C2in, C2out, C1in,
          ↪ C1out;
       electrical O11, O22, O12;
       parameter real PI44 = -136E-12;
       parameter real PIS = -488E-12;
       parameter real PID = -1556E-12;
       parameter real phi = 0; //CDF
       localparam real radphi = `M_PI
          ↪ /180*phi;
       analog begin
         I(C2in,C2out)<+(((PIS+PI44)/2*V
            ↪ (O11) + (PIS-PI44)/2*V(
            ↪ O22))*$pow($cos(radphi)
            ↪ ,2) + ((PIS-PI44)/2*V(O11
            ↪ ) + (PIS+PI44)/2*V(O22))*
            ↪ $pow($sin(radphi),2) +
            ↪ PID*V(O12)*$sin(2*radphi)
            ↪ )*I(C1in,C1out);
       end
endmodule
```

Code 1: Current controlled current source Verilog-A code *ncs_stress.va* from Fig. 4a.

APPENDIX B
CADENCE VIRTUOSO MODEL SETUP

Select the *ncs_stress.va* cell in Fig. 4a and click *Q*. Go to *CDF parameter of View* → *veriloga* and in the *phi* input prompt write *pPar("Angle")*. Do the same for the transistor width and length and write *pPar("Width")* and *pPar("Length")* in the respective input prompts. In the Virtuoso terminal go to *tools* → *CDF* → *edit*. Select *CDF Layer* as *base* and select the cell in Fig. 4a. Add "Width", "Length" and "Angle" rows and set them as "string" (Parse as CEL: yes, Parse as Number: yes).

ACKNOWLEDGMENT

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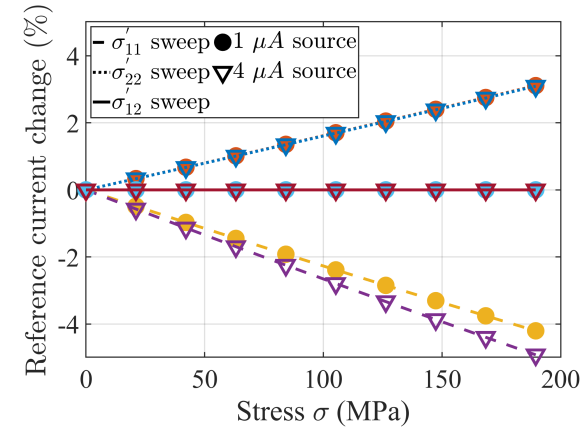
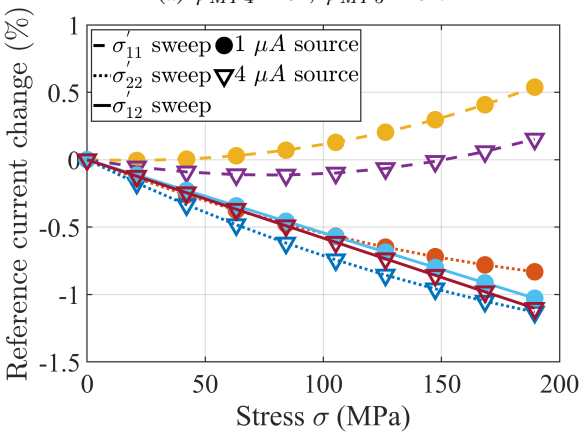


(a) $\varphi_{MP4} = 0°$, $\varphi_{MP5} = 0°$.



(b) $\varphi_{MP4} = 25°$, $\varphi_{MP5} = 25°$.

Fig. 8: Reference current source (Fig. 7) output current drift in response to stress. Dashed, dotted and whole lines represent the σ'_{11}, σ'_{22} and σ'_{12} stress sweeps respectively. Circles and triangles represent the I_1 (1 μA) and I_2 (4 μA) currents respectively.

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