Modeling of Electrical Properties of Al-on-Ge-on-Si Schottky Barrier Diode

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Abstract – In this work, different mechanisms that could cause degradation of the ideality factor in Al/Ge Schottky diodes on Si substrate are examined. Measured I-V characteristics of Schottky diodes have been fitted by the model of the diode developed in TCAD environment. The effects of Shockley-Read-Hall recombination parameters of epitaxial Ge on the I-V characteristics are simulated. The impact of interface traps on both Al/Ge and Ge/Si interfaces, as well as the effect of a buffer oxide layer on Al/Ge interface are analyzed by simulations providing a possible explanation for a degraded ideality factor in Al/Ge-on-Si Schottky diodes.

Keywords – aluminum, germanium, Schottky barriers, semiconductor defects, epitaxial growth, heterojunctions, Ge-on-Si

1. INTRODUCTION

In contrast to commercially available optoelectronic devices in III-V semiconductor materials, which are not technologically compatible with standard silicon CMOS processes, germanium epitaxy on silicon is offered as an ideal candidate for monolithic integration of both optical and electronic components [1]. Nevertheless, Ge-on-Si thin films could also be used as buffer layers for III-V epitaxy on silicon, which has already enabled the development of GaAs/Ge/Si monolithic tandem solar cells [2]. Various methods and techniques for integrating Ge devices on Si substrate have been developed and are mostly based on epitaxy [3].

Fabrication of stable and reliable metal contacts with n-type Ge has proven to be challenging and has therefore been the subject of numerous studies [4-8]. Most of the metals used for contacting the devices (Au, Cu, Ag, Pb, Ni, Al) form Schottky barriers to n-Ge with low donor concentration of up to $10^{16}$ cm$^{-3}$ [4]. Most of them form much higher barriers to n-Ge than it would be calculated from metal workfunctions and semiconductor affinities by applying the Schottky-Mott rule [4]. Furthermore, contacting of n-Ge with aluminum has been especially troublesome and remains partly unexplained. Whereas most references report relatively high Schottky barriers calculated from current-voltage characteristics (~0.5 eV – 0.7 eV) which could be attributed to Fermi level pinning [6,8], some papers report drastically lower values when calculated from C-V characteristics (~0.3 eV) [4]. In addition, time-dependent changes of the Schottky barrier height ($\Phi_B$) have also been measured in [9]. Finally, the value of Al/Ge Schottky diodes ideality factor is often reported to be in the range of 1.2 to 1.6, which should indicate either high values of SRH recombination currents, perimeter effects or the existence of some other physical mechanism which could significantly impact the current in forward bias. It has also been suggested that the increased values of the ideality factor could be explained by the formation of thin oxide on Al/Ge interface [5] or, more recently, by the formation of an inhomogeneous barrier [10]. Moreover, some authors have observed noticeable interdiffusion of germanium and silicon atoms upon Ge epitaxy and the existence of defective interface layers up to a few hundred nanometers thick [3], which could also deteriorate optoelectronic device properties. Some results show noticable Al migration through the epitaxial Ge, which could cause pitting of Ge and even Si substrate layers [11].

Different processes have been applied to improve the performance of Al/Ge contact, to depin Fermi level, pinned by defective interface states, and reduce the Schottky barrier, [6,8,12] However, the deposition of the thin layer of gallium and amorphous boron on the epitaxial germanium before the deposition of an aluminum electrode [3] has been proposed as a technology which could simultaneously provide better contact formation and ultrashallow doping of epitaxial Ge [13]. This method improves the performance of Al/Ge-on-Si photodiodes by significantly enhancing the ideality factor close to one. It has still not been fully explained what is the exact physical cause of ideality factor improvement, but characterization of a similar amorphous-B layer deposited on Si has shown formation of an interface hole layer (IHL) [14] which could directly impact the band structure of the device. In order to broaden the understanding of electrical properties of amorphous-B and Ga layers on the top of Ge, this paper presents an analysis of different mechanisms that could be the potential cause of a degraded ideality factor in Al/Ge-on-Si Schottky diodes.

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An analysis of Al/n-Ge Schottky barrier diode I-V characteristics has been performed by fitting the measured characteristics from [3]. The impact of different defective states on Al/Ge and Ge/Si interfaces in Al/Ge-on-Si Schottky diodes has been modeled in order to explain the contribution of each mentioned effect on current-voltage characteristics of the modeled diode.

II. EXAMINED STRUCTURE

The Schottky barrier diode has been modeled using Sentaurus TCAD software. Three different approaches to modeling the Schottky barrier on Al/Ge interfaces have been compared. The basic structure is shown in Fig. 1. Silicon substrate with 2 · 10^15 cm^-3 doping concentration has been defined, which corresponds to (100) 2-5 Ωcm phosphorous doped n-type Si wafer used in fabricated diodes [3]. The Philips unified mobility model has been used [15] in simulations [16].

On top of the silicon substrate, there is a 1 µm-thick layer of germanium. Germanium is grown inside 40x40 µm^2 oxide windows and doped by As. Material parameters used for simulations of germanium layer are mostly taken from [16]. One exception are mobility parameters where the Philips unified mobility model is used with parameters adjusted to the data found in [17]. Values of maximum carrier lifetime, for low-doped bulk Ge and for temperature of 300 K are $\tau_e = 10^3$ s and $\tau_h = 10^4$ s, for electrons and holes, respectively. Specific lifetime is calculated for every simulation node, depending on local dopant concentration. The other exception are emission velocities for calculation of thermionic current density which had to be calculated for the specific material. The density of thermionic emission current over the Schottky barrier equals to [18]:

$$J = A^* T^2 \exp(-q\Phi_b/kT) \left[ \exp(-qV/kT) - 1 \right],$$

where $A^*$ is the material-specific Richardson constant, $\Phi_b$ is the Schottky barrier height and $V$ is the external bias of the diode. The Richardson constant is defined as [18]:

$$A^* = 4\pi qm^*k^2 / h^3,$$

where $m^*$ is the carrier effective mass used for the density of states (DOS) calculations. The thermionic emission velocity, also called Richardson velocity, is given by [19]:

$$v_R = \sqrt{kT/2\pi m^*},$$

By combining equations (2) and (3), emission velocity can be calculated from the Richardson constant:

$$v_R = \sqrt{2qkT/h^3A^*}.$$
conduction mechanisms, such as Trap Assisted Tunneling (TAT), can contribute to the total current through the oxide, the model of the total current can be simplified to thermionic emission via extraction of the effective barrier height. This idea comes from the fact that most of the articles reporting barrier heights at Al/Ge interface extracted barrier values from $I-V$ characteristics, without modeling possible interface oxide formation. Thus, if any other conduction mechanism on the interface exists, it has already been summed up in the thermionic model defined by the effective height of the potential barrier. In addition to this, the physical properties of the possibly existing oxide layer are unknown, so the simulation model can finally be simplified to direct Al/Ge Schottky with the effective Schottky barrier height, which accounts for all of the mentioned physical effects (Fig. 3). However, the physical model presented in [5] predicts bias-activated deep traps in the interface oxide. Ionization of these deep states captures fixed charge in the oxide, which directly impacts the height of the barrier for electrons that are injected from Ge into the Al electrode. Therefore, the Al/Ge interface and the potential interface oxide have been finally modeled by simple Al/Ge contact, but with the field-dependent, variable Schottky barrier height.

III. RESULTS AND DISCUSSION

The simulated diode is modeled in order to fit $I-V$ characteristics from [3]. As TCAD simulation software predicts device currents per unit of the it’s length, all characteristic currents in this work have been multiplied to match the area of the measured diode. In this section, the different mechanisms that could possibly impact the diode current are analyzed. These mechanisms include traps at Al/Ge interface, traps at Ge/Si interface, perimeter effects and the formation of a buffer oxide layer between Al and Ge. Each mechanism is discussed as a possible cause of a degraded ideality factor and high values of extracted Schottky barrier heights compared to what is expected in light of the Schottky-Mott rule.

For the purposes of this analysis, the $I-V$ characteristics of the diode are divided into three different bias regions. Low-bias characteristics stand for the currents which correspond to bias values of less than 0.3 V. In this operation regime, the current is highly influenced by the Shockley-Read-Hall recombination process through the traps located in the depletion region. Mid-bias regime stands for regime in the vicinity of knee voltage, i.e. 0.3 V - 0.5 V. In this regime, the depletion region of the diode becomes narrower and the current is mostly defined by the barrier height for electrons at the Al/Ge interface, which directly corresponds to the Schottky barrier height. For higher voltages, the current is limited by the series resistance. Due to a very thin layer of epitaxial germanium and the corresponding higher carrier mobilities compared to Si, it can be assumed that the current in this region is mostly limited by the series resistance of a thick Si substrate. To reduce the size of the simulated structure, the area of the bottom-electrode equals the area of the diode. Therefore, silicon layer thickness has been varied in order to account for both contact resistances and collection of carriers by large-area bottom electrode.

A. Impact of Schottky barrier height

In the middle part of $I-V$ characteristics, the current of a diode is mostly determined by the height of the Schottky barrier on Al/Ge interface (Fig. 4). By increasing the barrier height, the mid-bias current is exponentially reduced, as expected from [1]. However, the Schottky barrier height had a significant impact on modeled characteristics for low forward bias. $I-V$ characteristics of the modeled diode for different values of the Schottky barrier height is shown in Fig. 4. The simulated characteristics show an abrupt rise around the origin due to the finite simulation step. Nevertheless, the ideal exponential part of the diode’s characteristics is proportionally reduced with a higher barrier. However, the slope remains constant. This implies that the value of the zero-bias Schottky barrier height should not have a significant effect on the diode’s ideality factor.

In order to fit the current for mid-forward biases, the modeled diode should have rather high values for barrier height (> 0.65 eV). To give these results some physical meaning, a comparison with literature can be made. As aluminum has a work function of 4.08 eV [21], and germanium an electron affinity of 4.00 eV [17], according to the Schottky-Mott rule, the barrier height in the conduction band should be $\Phi_B \approx 0.08 eV$.

However, different authors report calculations of Schottky barrier heights from $I-V$ characteristics of fabricated diodes to be significantly higher, e.g. $\Phi_B = 0.40 - 0.64 eV'$ in [4], $\Phi_B = 0.7 eV'$ in [6] and $\Phi_B \approx 0.6 eV'$ in [8]. Furthermore, when calculated from $C-V$ characteristics, the barrier height is
reported to be significantly lower, such as \( \Phi_0 = 0.34 \) eV in [4]. In addition to this, while the result of \( C-V \) based barrier height calculations has stable values, the size of the barrier determined from \( I-V \) curves shows aging properties [4-5].

If the Schottky barrier height was only 0.34 eV, as calculated from the capacitance, the barrier for electrons would barely exist. Thus, for Fermi distribution of carriers at 300 K, the contact would be ohmic and no rectification would be noticed. Interestingly, all of the Schottky diodes from [3] show rectifying behaviour and Schottky characteristics only when there is no final thermal annealing process applied. For those diodes where thermal annealing was performed after the deposition of the Al electrode, characteristics showed ohmic behaviour. This could possibly indicate breaking up of the oxide layer and establishing direct contact of Al and Ge – effective reduction of the Schottky barrier to lower values (Fermi level depinning), as such as measured from \( C-V \) characteristics. However, the extraction of Schottky barrier heights in [3] results in \( \Phi_0 = 0.65 \) eV, which would give a lower reverse saturation current and current for low-biases than measured on actual samples, as shown in Fig. 4.

**B. Impact of bulk and surface SRH recombination**

In order to increase the current at low biases in simulations and consequently degrade the ideality factor from ideal to the value of 1.24, as measured, the Shockley-Read-Hall doping-dependent recombination has also been included in simulations. If a high concentration of traps is assumed in the epitaxial Ge due to defective epitaxial growth directly on Si and the consequent formation of dislocations in the lattice, recombination in those traps could be the cause of ideality factor degradation. Furthermore, if recombination centers are located in the depletion region, the recombination component of the total current would likely have an ideality factor of up to 2, thus degrading the overall performance of the device. However, only by a significant boost of the SRH current component - by setting the bulk carrier lifetime of carriers to less than \( 10^{-8} \) s - the low-bias component of the current could be fitted (Fig. 5). However, for such low carrier lifetimes, the values of the reverse current would be significantly higher than as measured in reality. Furthermore, in the case of carrier lifetime being less than \( 10^{-8} \) s, mid-bias forward current is also increased. This effect could be reduced by using even higher values of the Schottky barrier (higher than 0.64 eV), which would inevitably reduce the current in the low-bias region. In addition, the effective carrier lifetime in Ge is reported to be in the range of \( 10^{-8} \)s [22] for wedge-cut unpassivated samples to \( 10^{-3} \) s for bulk material. [17] Due to the fact that it is not possible to boost bulk SRH recombination current exclusively in forward bias without overestimating the reverse current, and the fact that the effective lifetime values are significantly lower than those reported in the literature, it can be concluded that the modeling of Al/Ge interface with simple Schottky barrier and bulk SRH recombination is not sufficient to fit the measured characteristics.

**C. Impact of localized SRH recombination**

Another mechanism that could increase the recombination currents without over-estimating bulk Ge recombination parameters, is the introduction of additional recombination centers (traps) in specific regions of the device. Those are for e.g.: lattice dislocations, cracks in the epitaxial layer or grain boundaries, eventual presence of Al atoms deep in Ge layers or fixed charge ions. Simulation of mid-bandgap traps has been performed both at Al/Ge and Ge/Si interfaces. Traps are placed with Gaussian spatial distribution, with peak at the material interface and standard deviation of 200 nm. Characteristics of diode with additional deep-traps in the vicinity of Al/Ge interface is shown in Fig. 6. Simulations give results similar to those for

\[ \text{Distance from Interface (\text{nm})} \]

**Figure 8: Electric field at Ge/Si interface for different forward bias voltages for Schottky barrier diode with one-sided Gaussian fixed charge distribution at the Ge-side of the interface. Peak concentration of fixed charge is } N_{\text{CIF}} = 4 \cdot 10^{16} \text{cm}^{-3}. \text{ Spatial deviation of the distribution is } \sigma_{\text{dev}} \approx 200 \text{ nm. Interface depletion diminishes for larger biases.} **
simple increase of bulk Ge recombination parameters. The reason is in the fact that most of the deep-traps recombination centers are placed in the depletion region of the Schottky contact. Again, forward bias current is increased in low- and mid-bias regions, but also in reverse-bias region. The third possible cause of ideality factor degradation is recombination at Ge/Si interface. First Ge layers deposited on Si (100), up to 300 nm from Si/Ge interface, can contain dislocations due to significant strain and lattice mismatch of 4.2% between lattice constants of Ge and Si [3, 23]. Furthermore, strain at the interface could induce specific band alignment of Ge and Si, which could differ from expected alignment from heterojunction theory. [1, 24] If either heterojunction band alignments or defective Ge layer in the vicinity of interface could induce depletion at Ge/Si interface, poor ideality factor and also quite low reverse currents could be explained by the recombination in this secondary depletion layer.

The depletion region at the Ge/Si interface is firstly modeled by simple manipulation of material affinities (Fig. 7). It can be observed how low-bias current values are increased with wider depletion region at Ge/Si interface. No additional traps are needed to be simulated at Ge/Si interface, but just the basic depletion region. Increase of depletion region width at the interface increases low-bias forward currents, while at the same time preserves the values of forward mid-bias current. The reason is that the Ge/Si interface depletion region diminishes after forward biases larger than 0.2 V (Fig. 8). For biases under 0.2 V, Ge/Si depletion is dominant recombination center in the device and for larger biases it does not impact the current. The same effect is modeled without manipulation of material affinities, but with modeling of fixed charge mid-gap traps with Gaussian distribution at the Ge/Si interface. Peak values of fixed charge concentration are located at the interface and are marked in the legend of Fig. 9. Standard deviation of the distribution is 200 nm. The same effect of low-bias forward current increase, while preserving the values of mid-bias currents is achieved.

D. Impact of interface oxide formation

The next diode model, assuming the oxide layer at Al/Ge interface, has been simulated by utilizing two different approaches shown on Fig. 3. The first of them models the oxide as wide-bandgap semiconductor and defines the carrier transport as thermionic emission over the barrier in

Figure 9: I-V characteristics of the simulated diode for different peak concentrations of fixed charges on Ge/Si interface. The spatial distribution of traps is defined as Gaussian with peak on Ge/Si interface and standard deviation of 200 nm.

Figure 10: Reverse saturation currents for determination of zero-bias Schottky barrier height in field-dependent barrier model. The model still hasn’t been utilized which can be noticed from constant modeled reverse currents. SRH carrier lifetime is doping-dependent, with maximum set to low-doped bulk-Ge values, $\tau_{\text{SRH}} = 10^4$ s.

Figure 11: Ideality factors of a modeled diode with field-dependent model of Schottky barrier height (FDM) and another, with fixed charge on Ge/Si interface (peak concentration of $6 \cdot 10^{10} \text{cm}^{-2}$). Modeled diodes are compared with characterized Al/Ge-on-Si Schottky diode. Ideality factor of the equally processed Schottky diode, with additional Ga and B interlayers before sputtering of the electrode, is given as almost ideal reference (PureGaB). [3] Similar effects of ideality factor degradation can be achieved by modeling of Al/Ge interface oxide (red) or fixed charge on Ge/Si interface (blue).
them fully match in forward bias current and therefore have the same ideality factor. The diodes with area 40x40 μm² have ideality factor of 1.24, while those with area 6x6 μm², have ideality factor of 1.22. It could be assumed that perimeter effects which impact I-V characteristics should have larger effect on smaller diodes, due to higher perimeter to area ratio. In this case, measurements were showing the opposite. Possible explanation comes from the C-V curves [3] which show larger concentration of As dopant atoms in smaller diodes, especially in vicinity of Ge/Si interface. If there are defects, cracks in the crystal lattice, which could be modeled by fixed charge on Ge/Si interface, larger doping in epitaxial Ge layer would suppress their impact on current. If this is the case in diodes from [3], the impact of perimeter is presumed not to be dominant source of ideality factor degradation.

IV. CONCLUSION

In this work, different simulations of the impact of defective states on I-V characteristics of Al/Ge-on-Si Schottky diodes were performed. There are three possible causes of ideality factor degradation. The first one are acceptor traps in Ge near the interface with Al. Aluminum deposition could cause p-type doping of the Ge substrate or introduce other defects in the Ge lattice. The second possible cause could be the defective states at the Si/Ge interface, which induce the depletion region at the interface. This can be explained by strain due to a mismatch between Si and Ge lattice constants, which could introduce dislocations in the Ge lattice, up to a few hundred nanometers from the Si/Ge interface. Also, the presence of Al atoms deep in the Ge layer could be introduced during processing. The final explanation for performance degradation is the formation of an interface oxide between Al and Ge, which could induce voltage dependence of the barrier height and the ideality factor. Thermal annealing could possibly enable direct contact of Al and Ge, which would result in the reduction of the barrier height and the formation of ideal ohmic contact.

REFERENCES